University of Alberta

Tests of a Switched Capacitor Array for the ATLAS Calorimeter

By

Philip Issa Kayal

A thesis submitted to the Faculty of Graduate Studies and Research

in partial fulfillment of the requirements for the degree of

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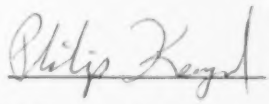

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Doug Gingrich

Dr. DM Gingrich

Dr. JL Pinfold

Dr. M Freeman

Dr. RI MacDonald

23 April 1996

to

my family

Abstract

This thesis describes an analog pipeline readout system that is being considered for the calorimeter of the ATLAS detector. Various tests have been performed on the switched capacitor array (SCA) chip, which is a crucial component of the analog pipeline readout system. In order to minimize the noise of the readout system, it is essential to know the noise of the various components of the system. The electronic noise of the SCA chip has been determined, and an analysis of the different contributions to the noise has been performed. When used in the ATLAS detector, the readout electronics will be subject to radiation. Thus, SCA chips have been exposed to electron, proton, and gamma radiation, and the performance of the chips under these conditions has been documented.

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CHAPTER 1

Introduction

The Large Hadron Collider (LHC), to be built at CERN (the European Laboratory for Particle Physics), Geneva, will allow physicists to study particles and their interactions at energies in the TeV range. There will be numerous new physics opportunities, including the search for a Higgs boson. Of course, a very complicated tool will be needed to detect these particles and to determine their properties. The proposed ATLAS (A Toroidal LHC ApparatuS) detector is such a tool.

The ATLAS Collaboration currently consists of about 1500 physicists and engineers, from over 140 institutions. The numerous development tasks have been divided amongst the participating institutions.

Many of the processes that physicists hope to study with the ATLAS detector are very rare. To compensate for this, the LHC will operate at a very high collision rate. This puts serious demands on the performance of the detecting equipment of ATLAS, as well as on the readout electronics that will transmit signals from detector elements. In order to fully exploit the high rate of the LHC, new electronics systems have been developed. Because all detector signals are processed by electronics, it is very important to use the most efficient, reliable and accurate readout system that can be attained.

One method of dealing with the high rate of the LHC is through the use of a pipeline, whereby signals from the detector are temporarily stored until a preliminary

analysis has been performed. Then, the signals are either discarded, or further analyzed. One scheme of pipelining detector signals makes use of a switched capacitor array (SCA) chip, which contains capacitors that store the analog charge collected from cells of the detector.

This thesis presents the pipelining scheme based on SCA chips, and also documents several tests which have been performed on these chips. These tests may be divided into two areas. A number of tests were conducted to determine the electronic noise of the SCA chips, and to analyze the components of the noise. Also, SCA chips have been irradiated, in order to determine their tolerance and response to various types of radiation.

It will be shown that a pipeline system which makes use of SCA chips is a viable solution to the ATLAS fast-electronics requirements.

CHAPTER 2

Physics Motivation

The major physics issues which will be studied at the LHC include the search for the Higgs boson, top-quark physics, B-physics, and a search for supersymmetric particles. The ATLAS detector is designed to examine all of these topics. As a general-purpose detector, ATLAS also has the capability of exploring physics beyond that discussed in this chapter, which demonstrates its tremendous physics potential.

2.1 Higgs Search

The Standard Model (of fundamental particles and their interactions) unifies the electroweak force and the strong force. The most prominent physics opportunity at the LHC is the search for the origin of spontaneous symmetry-breaking in the electroweak sector of the Standard Model. The existence of a neutral Higgs boson (H) is a possible manifestation of the spontaneous symmetry-breaking mechanism. One of the primary objectives of the ATLAS detector at the LHC is the discovery of the neutral Higgs boson and the subsequent investigation of its properties. Experimental searches for the Higgs boson present a major challenge to physicists. The mass of the Higgs boson is undetermined in the Standard Model, so one must be prepared to search over a mass range extending up to 1 TeV[1] and possibly beyond [1].

[1] By convention, mass units of eV/c^2 (where c is the speed of light in a vacuum) are simplified to eV.

For heavy Higgs bosons, $m_H > 2m_W$, the dominant decays are $H \rightarrow W^+W^-$ and $H \rightarrow ZZ$ so that the best place to look for evidence of the heavy Higgs boson at hadron supercolliders is in $pp \rightarrow VVX$ processes, where $V = W^{\pm}, Z$ [3].

For $180 < m_H < 800$ GeV, the most promising channel is the 4-lepton channel, $H \rightarrow ZZ \rightarrow 4\ell^{\pm}$, $2\ell^{\pm}2\nu$ (which have branching ratios of 0.0014 and 0.0088, respectively), even though the rate is very limited at the high end of the mass range. Here, the Higgs width grows rapidly, as do the momenta of the leptons to be measured. Therefore, the observation of a possible Higgs signal in this channel depends more on the luminosity than on detector performance. Previous studies [2] showed that a Higgs boson with $m_H \leq 800$ GeV should be detected in this channel for an integrated luminosity of 10^5 pb^{-1}. For larger Higgs boson masses, the event rate is too small to observe a clear signal, and to extend the range of observability would require an increased data sample. At lower masses the signal rates are high, such that with an integrated luminosity of 10^4 pb^{-1} a Higgs boson with mass between 200 and 300 GeV may be detected separately in the 4-muon and 4-electron channels.

On the other hand, the Higgs decay, $H \rightarrow W^+W^- \rightarrow \ell\nu q\bar{q}$, offers the possibility of exploiting the much larger branching ratio of about 0.20. In this case, however, there is a sizeable background from W multijet production where two of the QCD jets have an invariant mass close to m_W and fake the $W \rightarrow q\bar{q}$ decay [3].

For Higgs masses larger than the reach accessible to the 4-charged-lepton channel, the $H \rightarrow \ell\ell\nu\bar{\nu}$ channel may be considered. This channel benefits from a branching ratio which is at least six times greater, but the decay cannot be completely reconstructed because of the escaping neutrinos.

The decay $H \rightarrow \gamma\gamma$ is a rare decay mode. It is only detectable in a limited Higgs mass region where the production cross-section and the decay branching ratio

are both relatively large. It is the most promising channel for a Higgs search in the mass range $80 < m_H < 120$ GeV.

In order to search for the Higgs boson, the ATLAS detector must be able to probe many of these channels. This places considerable demand in terms of resolution on the detector elements, and on the readout electronics.

2.2 Top-Quark Physics

The rate of top-quark production at the LHC will be large, and will allow measurement of the top-quark mass in different channels. Even at the moderate luminosity expected during the first years of LHC operation (about 10^{33} cm^{-2}s^{-1}), roughly 10^7 $t\bar{t}$ pairs will be produced each year. The mass of the top-quark, m_t, may be measured by studying $t\bar{t} \rightarrow (\ell\nu b)(jjb)$ decays. $t \rightarrow jjb$ decays (where j represents a jet) will provide an abundant event sample, and will allow direct reconstruction of m_t, through the invariant mass of the 3-jet system. A high-p_T (transverse[2] momentum) lepton from the other top-quark decay will provide the trigger, which means that the lepton will be used to identify the decay. A few difficulties which must be handled are: background from other processes (such as fake electrons + jets, $b\bar{b}$ + jets, and W + jets), combinatorial background from the jets in $t\bar{t}$ events, and systematic uncertainties due to the detector and the theoretical models used [4, 5].

Despite the large signal rate, background from other processes must be considered. If the $t\bar{t}$ events are triggered on electrons, jets which fake the electron signature will cause a large background. To reduce multijet backgrounds well below the high-p_T electron signal, a rejection against jets of about 10^5 is necessary. The background

[2]Perpendicular to the beam axis.

from $b\bar{b}$ + jets can be reduced well below the $t\bar{t}$ signal using lepton isolation and missing transverse energy. The background from W + jets is of the same order of magnitude as the signal, and can only be reduced by requiring that at least one reconstructed high-p_T jet be tagged as a b-jet [6].

A signal-to-background ratio greater than one may be obtained by requiring that three jets with $p_T > 40$ GeV and $|\eta^3| < 2$ be reconstructed in the hemisphere opposite to the trigger lepton, that one of them be tagged as a b-jet and that the remaining pair have an invariant mass consistent with m_W.

Another way in which m_t may be accurately measured is through the use of multileptonic events from top-quark decays. Two leptons from the same top-quark decay would be used [7]. A third high-p_T lepton is required to minimize the background contribution. Thus, two leptons from W decay and one lepton from b-quark decay will form the signal sample for the mass measurement.

Searches for rare top-quark decays such as $t \rightarrow bH^+$ and $t \rightarrow Zc$ will also be performed. The decay $t \rightarrow bH^+$, if kinematically allowed, can compete with the $t \rightarrow bW$ decay, according to extensions of the Standard Model which include charged Higgs bosons [6]. The H^+ decays either to $\tau\nu_\tau$ or $c\bar{s}$. By requiring at least one isolated high-p_T lepton within $|\eta| < 2.5$, a large number of $t\bar{t}$ events may be obtained. The main background processes are $b\bar{b}$, W + jets, and combinatoric background from real and fake τ in $t\bar{t}$ events. The $b\bar{b}$ background will be reduced by imposing additional isolation cuts. The other contributions to the background will be reduced by requiring at least three reconstructed jets with $p_T > 20$ GeV and $|\eta| < 2.5$. Two of these jets will be tagged as b-jets.

[3]The pseudorapidity η is defined by $\eta = -\ln(\tan\frac{\theta}{2})$, where θ is the polar angle (the angle with respect to the beam axis).

Applying these selection cuts to $t \rightarrow bH^+$ decays would result in final states where an excess of events with one isolated τ (compared to events with an additional lepton) would be observed. It is expected that the signal from H^+ can be observed for $m_{H^+} < 130$ GeV.

Another rare decay of the top-quark, $t \rightarrow Zc$ (where c represents a charm quark), is expected to occur at a negligibly small rate in the Standard Model. This decay, if it is observed, would thus provide a glimpse of physics beyond the Standard Model. Also, this decay is of interest because a major source of background to events containing Z-boson pairs and jets is the decay $t\bar{t} \rightarrow ZZ + CC$[4]. For $t\bar{t} \rightarrow ZcWb$ with subsequent decays $Z \rightarrow \ell\ell$ and $W \rightarrow jj$, the signal would be identified as events with a reconstructed $Z \rightarrow \ell\ell$ decay accompanied by at least three jets with $p_T > 50$ GeV, one of which is tagged as a b-jet, and with one Z + jet combination of invariant mass within $\pm$ 8 GeV of m_t [6].

2.3 B-Physics

B-physics is a rich field, and the very large cross-section for b-quark production at the LHC will allow for a wide range of precision measurements. These include a study of CP violation[5] through the decays $B_d^0 \rightarrow J/\psi\ K_s^0$, $B_d^0 \rightarrow \pi^+\pi^-$, and $B_s^0 \rightarrow J/\psi\ \phi$. Also, a search for rare b decays such as $B_d^0 \rightarrow \mu^+\mu^-$ and $B_s^0 \rightarrow \mu^+\mu^-$ will be performed. Another interesting possibility is the measurement of B_s^0 mixing.

Much of the B-physics program will be performed during the first few years of LHC operation. B-physics studies will be experimentally easiest at the initial

[4]Charge conjugate.

[5]CP conservation implies that the behavior of particles is unchanged under simultaneous charge (C) and parity (P) transformations. Violations of CP conservation have been observed.

luminosity of about 10^{33} $cm^{-2}s^{-1}$, because pile-up[6] effects will be small, and the vertex detectors very close to the beam pipe will not yet be damaged by radiation.

The ATLAS detector is well-suited to perform a B-physics study, because of its powerful and flexible trigger system, high-resolution secondary-vertex measurement, and efficient track reconstruction and electron measurement down to low p_T [6]. The first level of triggering for B-physics requires a muon with a p_T threshold of 6 GeV and with $|\eta| < 2.2$. The second-level trigger reduces the rate by making a sharper p_T cut on the muon using the precision muon detectors and the inner tracking. Muons with $p_T \geq 5$ GeV and $|\eta| < 2.5$ can be identified in the external muon system. The vertex detector is capable of measuring B-decay vertices with a resolution of approximately 50 μm.

2.4 Supersymmetric Particles

Supersymmetric extensions of the Standard Model predict a large number of new particles, with masses and production rates such that the LHC is suitable for searching for these particles. The ATLAS detector would be able to discover such particles over a large fraction of the parameter space. It is expected that ATLAS will play a crucial role in either revealing or excluding supersymmetric extensions to the Standard Model.

In the framework of the minimal supersymmetric extension to the Standard Model, many possible signatures have been proposed for detecting supersymmetric particles. Some are very clean signals, but are significant in only a small region of

[6]Pile-up occurs when the signals from particles from different interactions overlap in the detector.

the available parameter space [8]. Three main signatures which would allow the exploration of a large fraction of the parameter space have been identified, namely multijets and missing transverse energy searches from squark/gluino production, same-sign dilepton searches from squark/gluino production, and three-lepton events from chargino/neutralino production [6]. Also, signatures in which a Higgs boson is present in the decays of squarks and gluinos have been studied [10].

2.5 Summary

The high energy and large collision rate of the LHC will provide a large number of physics opportunities. The ATLAS detector is designed to fully exploit the discovery potential afforded by the LHC. Thus, it must be able to explore all of the above physics issues with high precision. The precision with which results are obtained is arguably the most important design consideration of any detector. The readout electronics which process the signals from the various detector components must also operate with very high precision. The large collision rate and high energy of the LHC place challenging requirements on the readout electronics, and this thesis is concerned with a readout system which meets this challenge.

CHAPTER 3

The Large Hadron Collider

The Large Hadron Collider is a proton-proton collider, which will be installed in the existing 27 km circular LEP (Large Electron Positron) tunnel at CERN. It is expected that the center of mass energy of LHC collisions will be 14 TeV. Such a high energy is unprecedented in the world of particle colliders, and will undoubtedly provide a large number of physics opportunities.

The LEP collider is able to simultaneously accelerate electrons and positrons in opposite directions, using the same magnets. If the LHC were a proton-antiproton collider, it could employ a similar magnet system. However, it is very difficult to produce antiprotons, so this option is not viable. In order to collide two beams of protons, it is necessary to accelerate them in separate magnetic channels. To accomplish this, the LHC magnets will be twin bore magnets which have two separate beam channels within the same mechanical structure and cryostat. The superconducting dipole magnets will provide a magnetic field of 8.4 T.

There will be eight interaction points around the LHC ring. At each interaction point, the two beams of protons, which are circulating in opposite directions, will cross. Large, general purpose detectors (ATLAS and CMS (Compact Muon Solenoid)) will be placed at two of these interaction points.

Many of the physics processes that will be studied are very rare events. In order to obtain significant quantities of data of such events, a very large number

of total events must take place. Thus, it may be a problem to perform conclusive experiments in a reasonable amount of time. This dilemma will be avoided by having a large number of collisions per unit time. The design rate of proton bunch-crossings at the LHC is 40 MHz. Another characteristic of the LHC is a high luminosity, which is the number of particles per unit area per unit time. The design LHC luminosity is about 10^{34} $cm^{-2}s^{-1}$, although the initial luminosity will be lower.

CHAPTER 4

The ATLAS Detector

The ATLAS [6] detector is a proposed general purpose detector for the Large Hadron Collider, capable of exploring the new energy regime which will become accessible. The ATLAS detector would be fully operational at the startup of the new accelerator, and is designed to study a wide range of physics issues, such as top quark decays, B-physics, supersymmetry searches, and Higgs boson searches. The detector's versatility also demonstrates a potential to cope with unexpected new physics [9]. An isometric view of the ATLAS detector is shown in Figure 4.1.

The ATLAS detector is designed to fully exploit the discovery potential of the LHC. Thus, the ATLAS detector must be able to operate efficiently at the LHC beam-crossing rate of 40 MHz, and at the LHC luminosity of 10^{34} $cm^{-2}s^{-1}$.

It is important for any experiment to accurately identify particles and measure their energies. The ATLAS detector will provide signatures of electrons, muons and jets, as well as making high precision momentum measurements of charged particles. The magnet configuration is a crucial element that dictates the precision of the detector. An air-core muon magnet system and an inner superconducting solenoid will be used.

The ATLAS design consists of three main components: an inner detector, calorimetry, and muon detectors. The inner detector will perform tracking; the calorimetry will measure the energies of electrons, photons and hadronic jets; and the

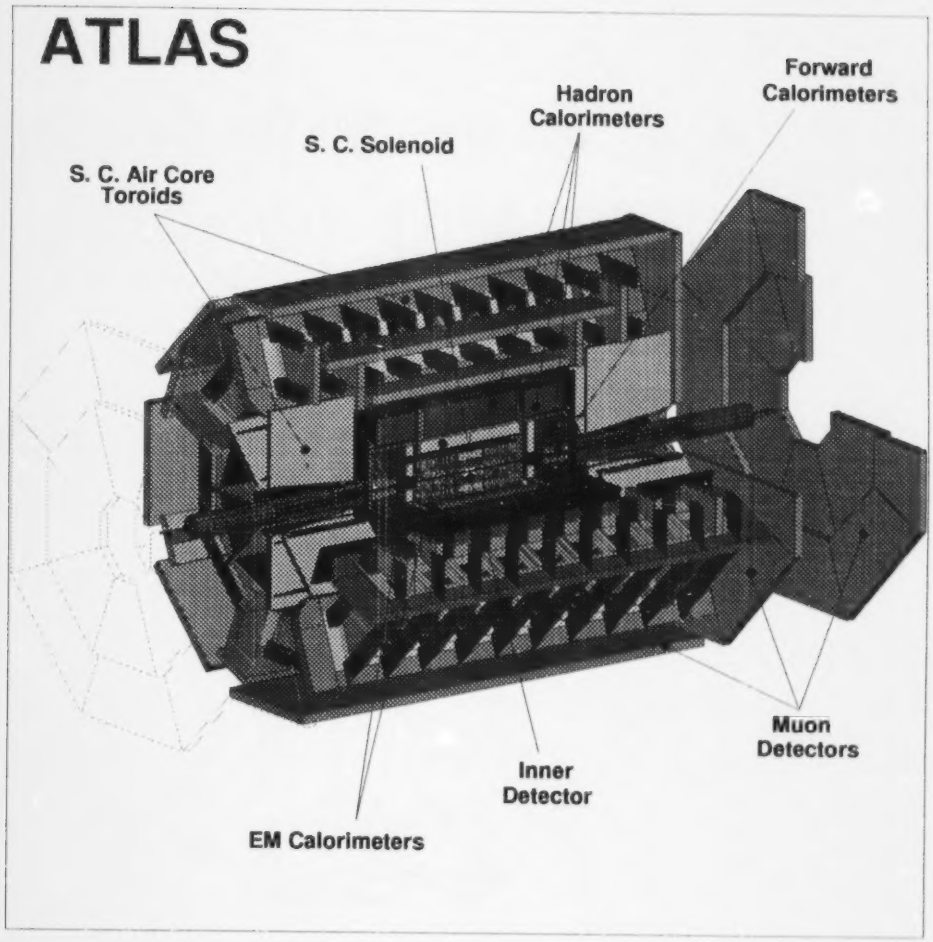

Figure 4.1: The ATLAS detector.

muon system will identify and make accurate momentum measurements of muons.

4.1 The Inner Detector

The principle aims of the central tracking system are to contribute to the detection and identification of leptons, photons (which have converted to electron-positron pairs) and hadrons over a large rapidity range, to measure high-p_T charged tracks, and to provide information for the second level of triggering [11].

The main requirements for high-luminosity operation include tracking coverage over the pseudorapidity range $|\eta| < 2.5$, tracking efficiencies of greater than 90%, electron-finding efficiencies of greater than 90%, tagging of b jets with a greater than 30% efficiency, and measurement of the z coordinate of primary vertices with at least four charged tracks to better than 1 mm [12].

The inner detector is very important for B-physics studies, because it provides a powerful and flexible trigger system, high-resolution secondary vertex measurement, and efficient track reconstruction and electron identification down to low p_T. As mentioned previously, B-physics studies will be easiest during initial lower-luminosity operation, because the pile-up effects would be small, and vertex detectors placed close to the beam pipe could survive for several years, before radiation damage occurs.

The inner detector consists of a barrel section between polar angles of 45° and 135°, and a forward section on each end. In the barrel region, the detectors are concentric cylinders, parallel to the beam axis, and in the forward part, they are "wheels" transverse to the beam axis. These geometries are intended to reduce the path length of particles through the material.

The general concept of the inner detector is to use a combination of a few

high-precision layers in the inner part of the tracker, and straw tubes in the outer part which supply a large number of measurements on the track trajectories [6]. This concept offers the benefits to pattern recognition of a device which makes a large number of "continuous" track measurements over a long track length, as well as those of a smaller number of higher-precision discrete points. In the barrel region, straw tubes provide continuous tracking, and semiconductor technology is used for discrete tracking. The semiconductor tracker (SCT) [13] consists of pixel detectors near the beam pipe, and silicon and GaAs strip detectors. In the forward regions, radial straw tubes are used for continuous tracking, and radial microstrip gas counters (MSGC) [14] provide discrete tracking. In order to measure and identify primary and secondary vertices, a semiconductor detector is placed close to the interaction point. Radiator material will be placed around the straw tubes and will detect transition radiation. Such a Transition Radiation Tracker (TRT) will assist in the identification of electrons.

Figure 4.2 shows the layout of the Inner Detector. It will fit inside the cryostat of the barrel electromagnetic calorimeter. A superconducting solenoid, integrated into the cryostat of the electromagnetic calorimeter, will provide a magnetic field of 2 T along the beam axis.

The choice of semiconductor technology in the barrel region of the inner tracker is determined by the location and intended function [6]. The outer detector layers (at radii of about 50 cm) have a large area and are made out of single-sided silicon microstrip detectors to reduce cost. The detector layers at radii of 20 and 30 centimeters are close to the vertex, and so should consist of a small amount of material to minimize bremsstrahlung effects. This can be achieved by using double-sided silicon microstrip detectors. The innermost detector layers, at radii of 11.5 and 14.5 centimeters, are composed of silicon pixel detectors which provide point information

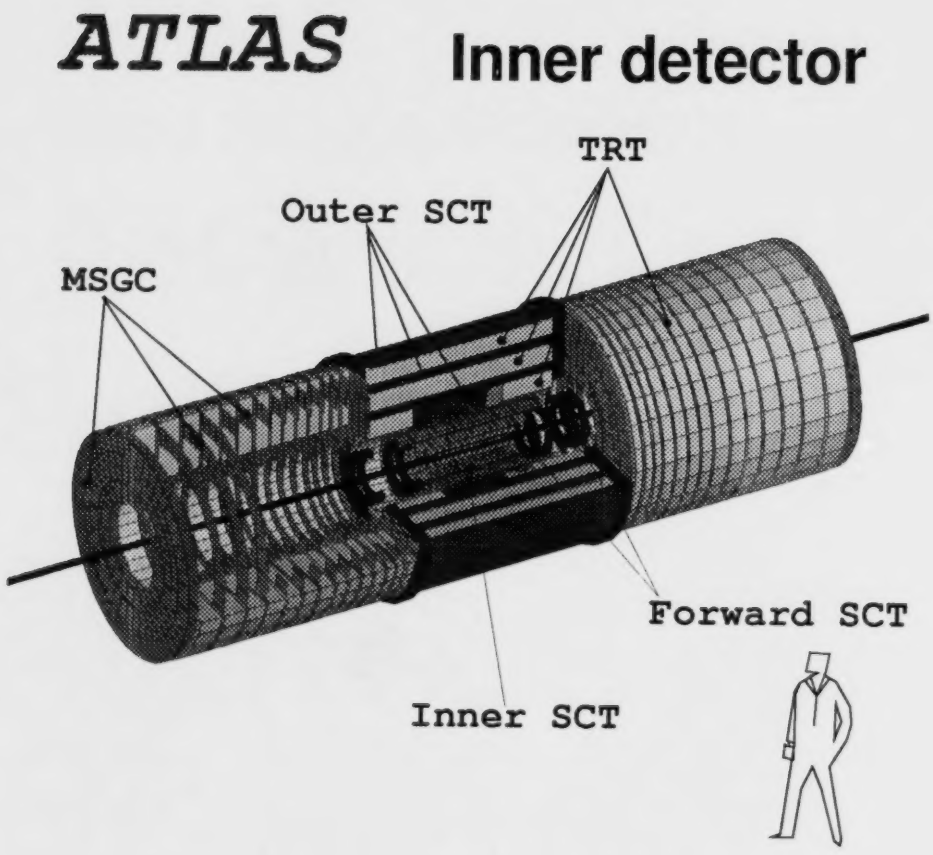

Figure 4.2: Three-dimensional cutaway view of the ATLAS Inner Detector (taken from the ATLAS Technical Proposal, 1994).

close to the vertex.

The design of the Inner Detector is influenced by physics requirements, environmental constraints, and overall cost. The Inner Detector Collaboration has concluded that the best compromise between these requirements is to use three technologies: semiconductors, microstrip gas counters, and a straw tracker with transition radiation enhancement.

4.2 Calorimetry

Calorimeters will be one of the most essential components of the detectors at the LHC. The main purpose of a calorimeter is to measure the energy and position of the particles which pass through it. This is done by sampling the energy deposited by the showers in the calorimeter. Some of the goals of ATLAS calorimetry are: efficient identification of photons and electrons in the energy range from 10 GeV up to a few TeV, hermetic jet and missing energy determination, effective triggering, and the ability to withstand the radiation level of the LHC [6]. A three-dimensional view of the ATLAS calorimeter system is shown in Figure 4.3.

The calorimetry consists of two types: lead/liquid argon (LAr) electromagnetic (EM) calorimetry, and hadronic calorimetry. The main calorimeter system covers $|\eta| < 3.2$. The calorimeter system can be divided into three parts, both geometrically and mechanically: a barrel part and two end-cap parts, one on each end of the barrel. The barrel and end-cap sections both consist of LAr EM calorimeters, followed by hadronic calorimetry which is thick enough to fully contain the very high energy jets produced by the LHC. The EM calorimeters will detect electrons, positrons and photons. The hadronic calorimeters will detect hadrons which pass through the EM

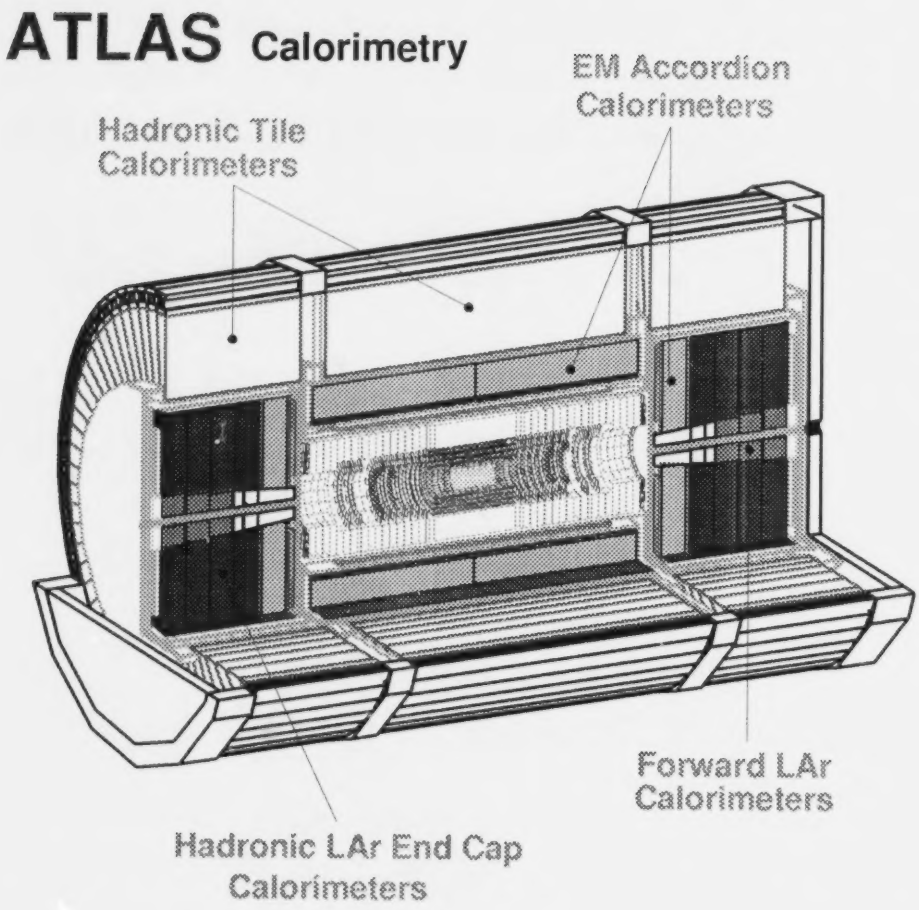

Figure 4.3: Three-dimensional view of the ATLAS calorimeter system (taken from the ATLAS Technical Proposal, 1994).

calorimeters. Neutrinos will not be detected by the calorimetry.

Calorimeters are also used to determine if there is missing transverse energy, which would signify the presence of undetected particles, such as neutrinos. Thus, full coverage is important, and so the calorimetry must extend to very small angles from the beam direction. To accomplish this, in the region $3.1 < |\eta| < 4.9$, forward calorimeters [15, 16] (both EM and hadronic) will be used. Because they must be placed very close to the beamline, the forward calorimeters must be significantly more radiation hard than the other calorimeters. This requires that a denser calorimeter be used. The forward calorimeter design consists of rods and tubes within an absorber matrix. Each rod is supported inside a tube by means of a quartz fibre, as shown in Figure 4.4, to form an electrode. The tubes are made of stainless steel. Liquid argon will fill the narrow gap between the inner diameter of the tube and the outer diameter of the rod. These electrodes will be placed in a hexagonal pattern within an absorber, with the electrode axes parallel to the beam line. Each of the forward calorimeters consists of three modules: an EM module, followed by two hadronic modules. The EM module will be made of copper, while for the two hadronic modules, the rods and matrix will be made of a tungsten alloy. The forward calorimeters will be integrated into the end-cap calorimeters, at a distance of about 5 meters from the interaction point.

In front of the barrel EM calorimeter will be placed the superconducting solenoid, which is designed to provide an axial magnetic field of 2 T at the center of the calorimetry. In order to minimize the amount of material present, the coil is designed to be as thin as possible, and also the vacuum vessels of the solenoid and barrel calorimeter will be combined.

There are three independent cryostats: a barrel cryostat and two end-cap

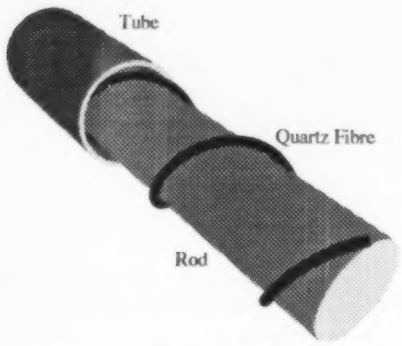

Figure 4.4: Exploded view of the tube electrode structure of the forward calorimeter (taken from the ATLAS Technical Proposal, 1994).

cryostats. The barrel cryostat contains the barrel EM calorimeter and the solenoid. Each end-cap cryostat contains the EM and hadronic end-cap calorimeters as well as the forward calorimeter. Each cryostat consists of two aluminum alloy vessels. The inner vessel is called the cold vessel and maintains the liquid argon at a temperature of 89 K. The outer vessel is called the warm or vacuum vessel and isolates the cold vessel from the outside. Superinsulation will be placed between the two vessels.

4.2.1 Electromagnetic Calorimetry

The liquid argon technology was chosen for the EM calorimeter because it is radiation hard, and allows easy segmentation of the calorimeter into small cells, thus reducing pile-up. Argon has very good charge transport properties, however a drawback is the necessity of cryogenics. The RD3 Collaboration has made significant progress in designing and testing LAr EM calorimetry, based on the accordion concept [17].

In order to facilitate the efficient reconstruction and identification of electrons and photons, a LAr pre-shower detector was to be placed between the EM calorimeter

and the cryostat coil assembly, in both the barrel and end-cap regions. However, a cheaper and simpler approach will be employed, in which the first sampling of the EM calorimeter is segmented into very thin strips, and so may serve as a pre-shower device. The simplest arrangement has the strips narrow in η, providing a one-dimensional measurement.

The LAr EM calorimeters consist of plates of lead separated by liquid argon. A potential difference will exist across the LAr gaps. A charged particle passing through the liquid argon will ionize it, freeing electrons. These electrons will then drift towards the positively charged side of the LAr gap. This will produce a current, which can be amplified and measured. In reality, as say an electron passes through a calorimeter, it will shower. This will result in a large number of ionized tracks in the calorimeter. The total of all of the measured currents will be proportional to the total energy of the incoming particle. The LAr EM calorimeters will also detect photons, because as photons pass through the calorimeters, they will free electrons, which will then shower. The geometry of the LAr EM calorimeters is based on the accordion concept, and is shown in Figure 4.5.

Because lead is much denser than liquid argon, most of the incident particle's energy will be deposited in the lead plates. The lead is necessary to prevent any of the energy from escaping from the calorimeter and hence avoiding detection and measurement. But because of this, only a small amount of the incoming energy will actually be deposited in the liquid argon, and subsequently measured by the calorimeter. Thus, the LAr EM calorimeters only sample the energy of the shower periodically (in depth). By using many sections of liquid argon, one can obtain a high sampling frequency. Although such a calorimeter may only measure a small amount of the total energy deposited (typically about 10%), once the calorimeter has been calibrated, one can determine the total incoming energy.

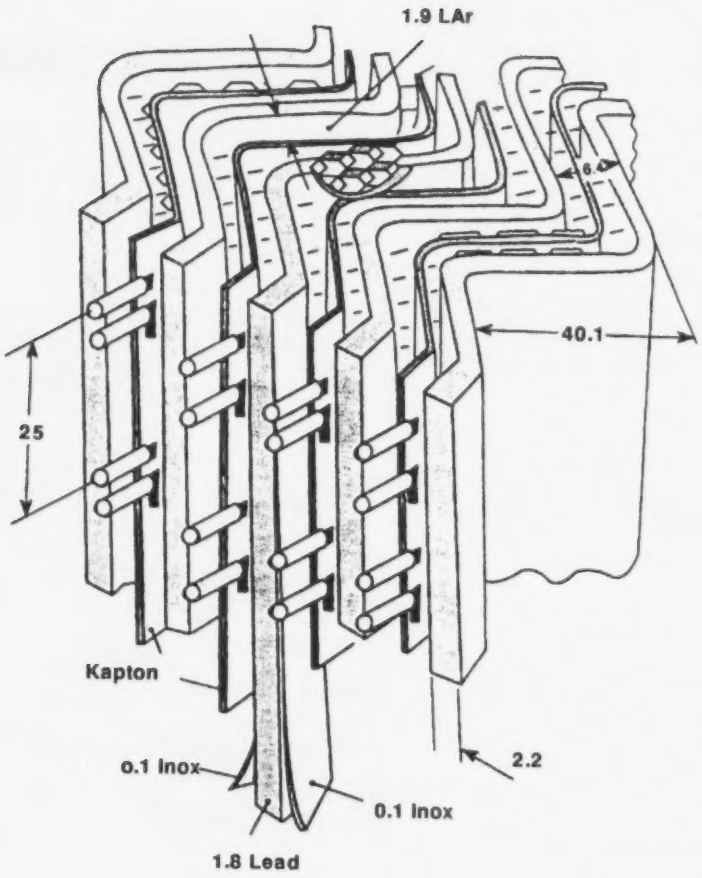

Figure 4.5: Artist's view of an accordion calorimeter.

The energy resolution of electromagnetic calorimeters can be expressed as the quadratic sum of three terms: $\frac{\Delta E}{E} = a\% \oplus \frac{b\%}{\sqrt{E}} \oplus \frac{c\%}{E}$. The first term is the constant term, which does not vary with energy. It effects the energy resolution most at high energies, and is due to imperfections (such as non-uniformity) in the calorimeter construction and in the purity of the liquid argon. The second term is called the sampling term, and is inversely proportional to the square root of the energy. Thus, as the energy increases, the contribution from this term decreases. The sampling term can be reduced by increasing the sampling frequency. The third term in the energy resolution is due to electronic noise and pile-up, and is inversely proportional to the energy. Again, an increase in energy will reduce the contribution from this term. This third term is the one which is of concern to this thesis, and should be lower than the other terms over most of the energy range. It is expected that a constant term of less than 1% and a sampling term of less than or equal to $10\%/\sqrt{E}$ would satisfy the goals of the ATLAS EM calorimetry.

Thus, we can see an important characteristic of both electromagnetic and hadronic calorimeters - the energy resolution improves as the energy increases.

4.2.2 Hadronic Calorimetry

The primary purposes of the hadronic calorimetry in ATLAS are to identify jets and measure their energy, and to determine missing transverse energy [6]. Hadronic showers are detected with a poorer resolution than for EM calorimeters, partly due to the fluctuations in the amount of energy lost to nuclear binding energy effects. The energy resolution of a hadronic calorimeter is given by three terms, added in quadrature: $\frac{\Delta E}{E} = \frac{a\%}{\sqrt{E}} \oplus b\% \oplus \frac{c\%}{E}$. The first term is called the sampling term, and is due to the geometry of the calorimeter. The sampling term is proportional to

the inverse of the square root of energy. The second term is a constant term, which is due to imperfections in the construction and materials of the calorimeter, and also will have a contribution from an unequal response of the calorimeter to electrons and hadrons. The constant term is most significant at high energies. The third term is due to electronic noise and pile-up.

In the barrel and end-cap regions, hadronic calorimetry with an energy resolution of $\frac{\Delta E}{E} = \frac{50\%}{\sqrt{E}} \oplus 5\%$ should be sufficient to meet the goals of the ATLAS detector. In the forward region, an energy resolution of $\frac{\Delta E}{E} = \frac{100\%}{\sqrt{E}} \oplus 10\%$ should be adequate.

The hadronic barrel calorimeter is the only part of the calorimetry system which is not based on an absorber/liquid argon scheme. It will consist of scintillating tile, with steel as showering material. The tiles will be staggered in depth and oriented perpendicular to the colliding beams.

The hadronic end-cap calorimeter will consist of copper absorbers, with liquid argon as the ionization material. It will cover a range of $1.5 \leq |\eta| \leq 3.2$. Each end-cap consists of two wheels of similar construction. Each wheel is made of sheets of copper absorber, separated by gaps for the liquid argon.

4.3 The Muon System

The toroidal magnet configuration of ATLAS allows the muon identification and triggering to take place entirely outside of the calorimetry. Because the toroidal system will itself provide a measurement of momentum, the muon detection and triggering system is capable of operating up to the design luminosity of the LHC, 10^{34} $cm^{-2}s^{-1}$, and above.

The superconducting air-core toroid system is designed to produce a large-volume field with an open structure giving easy access for the installation of muon detectors. The barrel magnet, covering the central region up to $|\eta| = 1.2$, provides a magnetic field length of 3 Tm. This magnet consists of eight separate superconducting coils assembled as an axially symmetric array around the 10 meter diameter calorimeter barrel. Each coil is of a flat "race track" configuration, extending over a surface area of 26×5 m^2. The coil is made of two single "pancakes" wound and clamped rigidly on both sides of a cold solid plate which acts as a central web to contain the internal forces imposed on the conductor. The pancakes are made of 50 turns of aluminum-stabilized rectangular conductor.

The forward regions are covered by two smaller end-cap toroids, which are designed to extend the coverage of the superconducting magnet system to about $|\eta| = 3$. These end-cap toroids will provide a magnetic field length of 8 Tm at $|\eta| = 2.8$. Like the barrel, each end-cap toroid consists of eight coils. The end-caps fit inside the barrel, the coils of the end-cap fitting between the coils of the barrel at the same radius [6].

A muon track is always measured in three "points", from which the momentum can be determined. In the barrel, one point is in front, one behind, and one in the middle of the magnetic field region. In the end-caps, one point lies in front, and two lie behind the magnet. In the ATLAS detector, each point will be represented by a number of tracking chamber layers, forming a superlayer. The tracking system will provide a coordinate measurement in the bending plane with a resolution of 100 μm or better per superlayer. Figure 4.6 shows the location of the muon tracking chambers.

In the barrel region, the muon chambers are arranged in cylindrical shells, concentric with the beam axis. Each chamber consists of two multilayers of drift

tubes. Most of the barrel chambers are rectangular in shape. In the end-cap region, the muon chambers are mounted vertically. Neighbouring chambers will overlap for full azimuthal coverage. The end-cap chambers are of trapezoidal shape.

A separate muon detector system is used for triggering. For Higgs searches and B-physics, a high single-muon trigger efficiency is required. The trigger scheme is based on a coincidence logic, to combine the muon trigger with the other subdetector triggers for the same bunch-crossing. The muon trigger system uses two types of detectors: Resistive Plate Chambers (RPCs), and Thin Gap Chambers (TGCs). The same system also provides the second-coordinate measurement necessary for pattern recognition and momentum reconstruction.

The muon trigger system in both the barrel and end-cap regions consists of two stations of detectors [18]. The first station (S_2) is split into two substations, each of which is made of two layers of strip detectors. The second station (S_3) consists of three layers. A schematic diagram of the locations of the muon trigger stations is shown in Figure 4.7.

4.4 Triggering

Because most of the collisions that take place will not be ones that are interesting in terms of physics content, many of the bunch-crossings will be discarded. In order to accomplish this, each bunch-crossing will be subject to tests which determine if the bunch-crossing warrants further analysis or not. Such tests involve checking to see if certain particles and/or energies were detected. Each of these tests is called a trigger condition. The ATLAS trigger architecture is shown in Figure 4.8. The first rough check that takes place is called the Level 1 trigger.

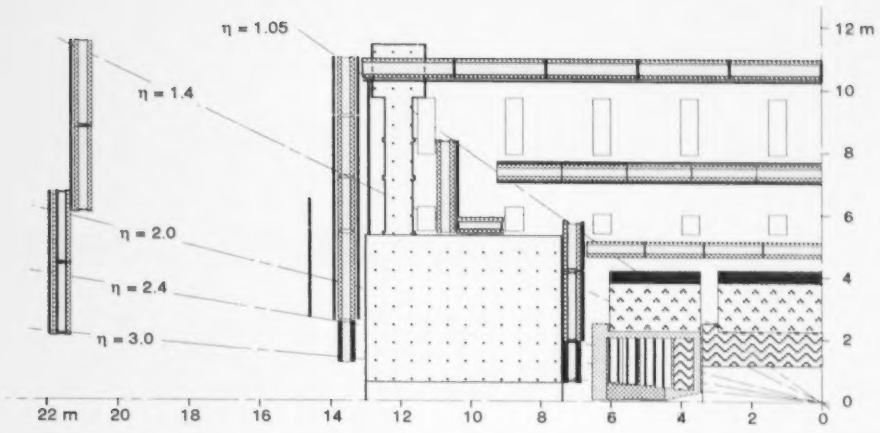

Figure 4.6: Side view of the detector, showing the position of the muon chambers (taken from the ATLAS Technical Proposal, 1994).

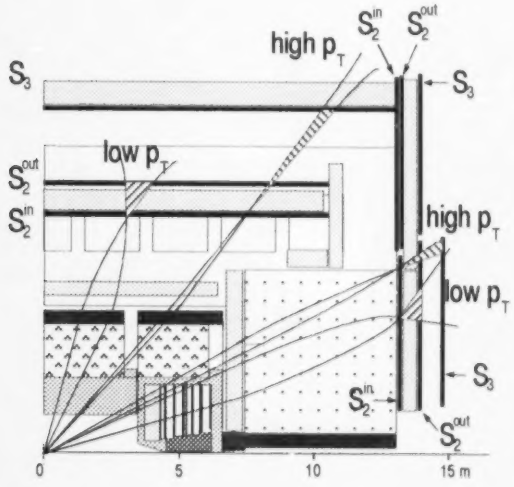

Figure 4.7: Schematic of the muon trigger in the barrel and end-cap (taken from the ATLAS Technical Proposal, 1994).

The design LHC bunch-crossing frequency is 40 MHz. The latency of the Level 1 trigger will be about 2.5 μs, during which time the data from all detectors will be stored in analog or digital pipeline memories until the first-level decision is made. The latency of the Level 1 trigger is the amount of time that elapses from when the LHC bunches cross until the trigger decision reaches the front-end electronics. The Level 1 trigger is expected to select events at a mean rate of about 100 kHz. This means that the readout system has on average 10 μs to read data from the front-end electronics before the arrival of the next trigger accept. The Level 1 trigger will be determined by the calorimetry and/or the muon system information.

A second-level trigger will further reduce the rate, by demanding additional event signatures [19]. The inner detector may be used to achieve the desired background reduction, by locating tracks and determining their p_T. The Level 2 trigger architecture is based on the use of Regions of Interest. The regions of the detector containing interesting features (such as high-p_T electromagnetic clusters (electrons/photons), jets or muons) are identified by the Level 1 trigger system. The Level 2 trigger then accesses and processes data from only these regions, which is a small fraction of the total detector data. The Level 2 trigger is designed to have an input rate of up to 100 kHz, and an output rate of 1 kHz.

The third-level trigger will perform the final event selection and data reduction prior to mass storage. Event selection for calibration and physics analysis, started at the second level, will be refined at the third level. In order to achieve full event analysis, an event builder will merge all of the data into complete events. The Level 3 trigger could use fully calibrated data and run offline-type algorithms.

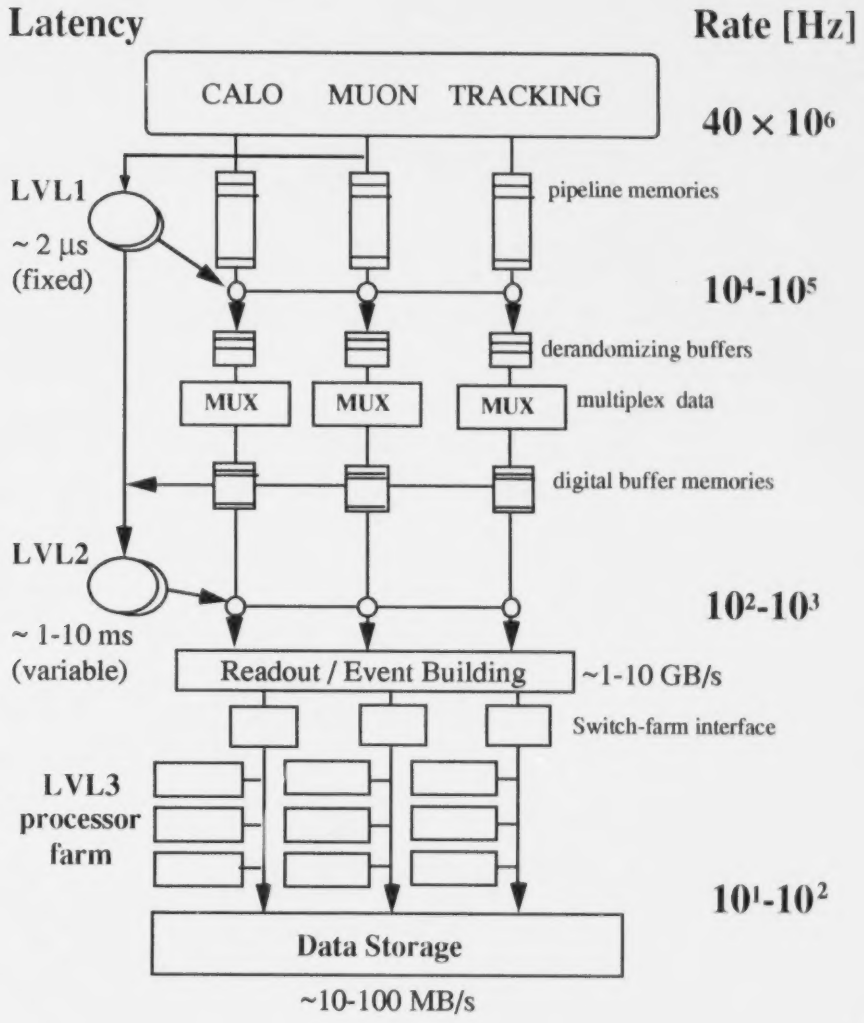

Figure 4.8: The ATLAS three-level trigger architecture (taken from the ATLAS Technical Proposal, 1994).

CHAPTER 5

Calorimeter Electronics

This chapter presents an overview of the front-end readout electronics for ATLAS calorimetry. In particular, the scheme of pipelining detector signals is discussed.

5.1 Front-End Electronics

It is intended that the readout electronics have a 16-bit dynamic range. The dynamic range of the readout system is determined by the energy deposited in the calorimeter. It is estimated that a single calorimeter cell will experience a maximum energy deposit of 2 TeV. The requirement of a 16-bit dynamic range dictates a least count of 32 MeV. This is smaller than the expected preamplifier noise.

For the calorimeter components which utilize liquid argon, the front-end electronics begin with electrodes which collect the signals from the liquid. Printed circuit motherboards will combine the signals from 3 or 4 electrodes to form single readout channels. The motherboards also hold the cryogenic preamplifiers and distribute calibration signals.

Figure 5.1 shows the drift current versus time for an ionization calorimeter, and the response of a bipolar shaper with a shaping time[1] of 20 ns. Calibration circuits provide a precise pulse, simulating the triangular signal from the detector,

[1]The shaping time is about half of the peaking time (5 to 100%) for a triangular signal from the detector, and is defined as the peaking time for a delta pulse [20].

and allow precise measurements of the amplitude and timing for each channel. The calibration signal must have a very sharp edge (about 1 ns) and an accurate initial value. The decay time should be equal to the electron drift time (about 400 ns).

The purpose of the ASIC (Application Specific Integrated Circuit) shaper chips is to clip the long (400 ns) decay of the detector signals, and to optimize the signal-to-noise ratio. The shaping time is chosen to minimize the total noise, which is a combination of electronic noise and pile-up noise. This requires shaping times of between 20 and 50 ns for the various calorimeters at full luminosity. A multiple sampling technique (combining 3 to 5 samples) can be used to provide an optimum noise response [21].

Preamplifiers amplify the small calorimeter signals to minimize the noise from pick-up and from the subsequent stages. The preamplifiers determine the ultimate noise performance of the readout system, which must be optimized in order to achieve good resolution at low energy [6].

In the barrel region, noise considerations require that the liquid argon preamplifiers and calibration circuits be located within the cryostat. Silicon preamplifiers have been shown to be radiation hard, and reliable at cryogenic temperatures. Motherboards will be mounted directly on the calorimeter. Feed-throughs will carry the calorimeter signals through the cryostat walls. The preamplified signals will then be transferred to signal shaping electronics which will be placed as close as possible to the feed-throughs. In the end-cap regions, high radiation levels and a lack of space require that the preamplifiers be located outside of the cryostat, approximately 5 meters away. This is called the "0T" scheme, because there will be no transistors within the cryostat. The noise performance is comparable to levels achieved with cryogenic silicon preamplifiers.

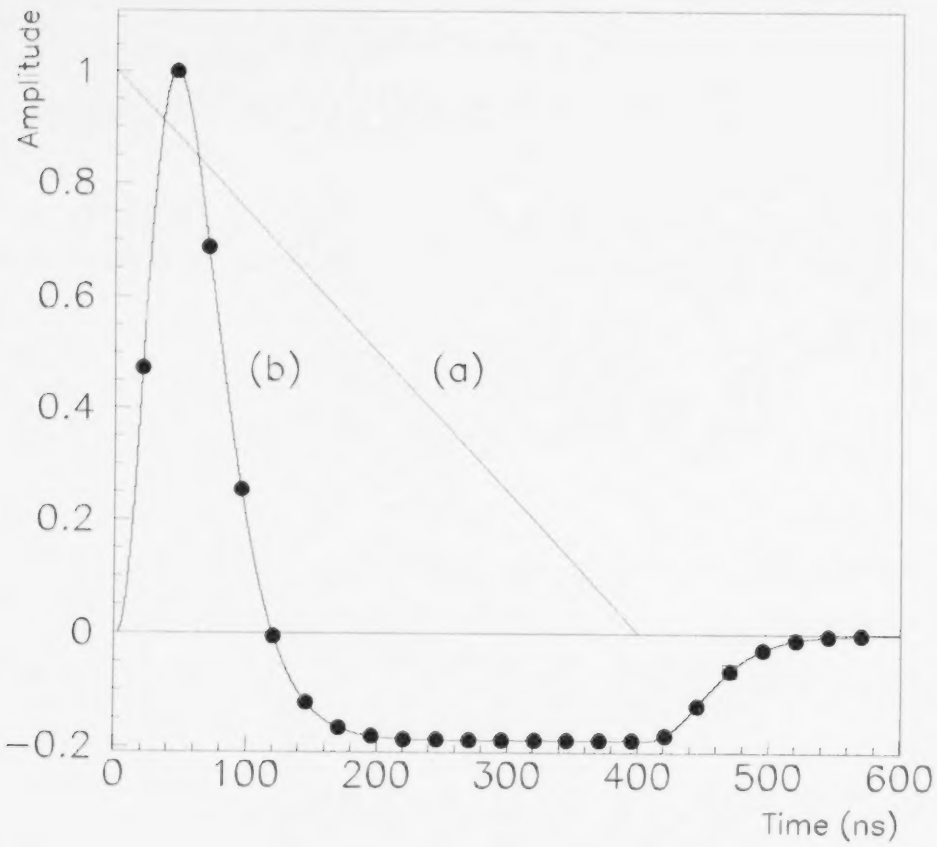

Figure 5.1: (a) Drift current versus time for an ionization calorimeter; (b) Response of a bipolar shaper with a shaping time of 20 ns. The dots indicate the beam crossings. (Taken from the ATLAS Technical Proposal, 1994.)

A dual-range scheme is employed in order to obtain a 16-bit dynamic range while using a readout system capable of only a 13-bit resolution. The shapers will split the signals, and amplify one of the split signals by a factor of about 16, to obtain a low gain channel. The other unamplified split signal will be a high gain channel. The shaper chips will each be responsible for eight calorimeter channels, and will be mounted directly on the pipeline boards.

A trigger tower is formed by summing the signals from a group of calorimeter cells. The shaper circuits will provide some of the analog sums required to form the Level 1 trigger towers, because they will be assigned to adjacent calorimeter cells in the same longitudinal depth. The pipeline boards will transmit the sums to a Level 1 trigger summation board, for further summing to form the trigger towers.

5.2 Readout Electronics

The readout electronics are responsible for forming the Level 1 trigger sums, storing the analog signals until a Level 1 trigger accept, and digitizing the accepted events.

It is intended to use a common readout technology for the barrel, end-cap, and forward calorimeter subsystems. This will reduce development efforts and improve integration with a uniform, cost effective architecture.

In order to provide a deadtime-free Level 1 trigger, the readout electronics for all of the calorimeter subsystems must sample the signals from each calorimeter cell at the LHC bunch-crossing rate of 40 MHz. A combination of these signals is sent to the Level 1 trigger. The latency of the ATLAS Level 1 trigger will be about 2.5 μs, so the individual calorimeter signals must be stored temporarily in a pipeline until a decision from the Level 1 processor has been received. The pipeline will have 256

storage cells (capacitors) per input channel. About 100 storage cells will be occupied by data which are awaiting trigger decisions, and the other 156 cells will form a buffer containing accepted data which are awaiting digitization.

If a bunch-crossing is selected by the Level 1 trigger as being desirable, the calorimeter signals are digitized and then processed. The energy deposition, timing, and pile-up correction are extracted from the signals. This information is then passed on to the next level of triggering, which is the Level 2 trigger.

As mentioned previously, the front-end electronics are located on the detector. In order to minimize data transmission, the Level 1 trigger signals and the data extraction are done on the detector also.

A 16-bit dynamic range, with a sampling frequency of 40 MHz, is not easily obtained using current technology. To meet these criteria, two independent approaches are being studied.

5.3 Digital Pipeline Approach

One readout scheme being studied is a digital pipeline. This involves digitizing the signals from individual detector elements for each bunch-crossing. The data would then be stored in a digital memory until a decision is made by the Level 1 trigger.

The advantage of this approach is that the analog signals would be digitized immediately, before they are degraded by the noise of the systems. This could be done very close to the calorimeter, and so very little resolution would be lost due to noise.

The disadvantage to a digital pipeline is that the digitizer must operate at

a very high speed, since the sampling frequency is 40 MHz. This is difficult to accomplish with a 16-bit dynamic range. Range compression schemes may be used together with 10-bit or 11-bit ADCs. Input signals, with a dynamic range of 15-16 bits, are compressed and digitized at sampling frequencies up to 80 MHz. The resulting 10-bit data are linearized and expanded to the full 16-bit dynamic range by means of a look-up table containing the inverse transfer function of the detector-electronic chain. This provides an absolute calibration for each individual channel.

An example of a digital pipeline approach is the Front-End and Readout MIcrosystem (FERMI) system, developed as RD16 [22]. This is a complete readout system which incorporates into a single multichip module a dynamic range compressor, an ADC, non-linearity correction, generation of Level 1 trigger data, digital signal processing, data buffering, and a local controller [6].

An amplifier with four ranges of gain will process the detector signals, which have a dynamic range of up to 16 bits. The resulting analog signals are converted to digital signals by 10-bit ADCs. Prototype digitizers have operated at rates greater than 40 MHz. The 10-bit data are then linearized and re-expanded to 16 bits. Each FERMI module is expected to be responsible for 8 or 16 detector channels.

5.4 Analog Pipeline Approach

Another type of system being considered is an analog pipeline. This approach involves storing the analog charge from each detector element in capacitors, while a Level 1 trigger decision is being made. The signals from the successive bunch-crossings would be stored in different capacitors. The capacitor addresses associated with each bunch-crossing would be recorded digitally. If the Level 1 trigger accepts the bunch-crossing,

then the signals from that bunch-crossing are digitized. Once the data have been read, the capacitors may be overwritten by a subsequent bunch-crossing. Since only a small percentage of the bunch-crossings are accepted, this method greatly reduces the required digitization rate. Thus, an analog pipeline system has the advantage of placing a reasonable demand on the digitizing electronics.

The disadvantage of this approach is that the analog signals must be stored for several microseconds, with high precision. Since the electronics will be in a noisy environment, this will result in significant noise pickup, which will reduce the dynamic range.

A prototype analog pipeline readout module is currently being tested at the University of Alberta. The readout module and the tests performed form the topic of this thesis.

CHAPTER 6

An Analog Pipeline Readout System

As discussed above, an analog pipeline is one of the approaches being considered for the readout electronics of the ATLAS calorimeters. The entire readout system must have a 16-bit dynamic range, with a 12-13 bit accuracy. Also, it must have low power requirements, low cost, operate with no deadtime, and be compact, reliable and radiation hard.

6.1 Pipeline Readout Board

It will be challenging to obtain a digitization rate at the LHC bunch-crossing rate of 40 MHz with a greater than 15-bit dynamic range. However, it is possible to use a digitization rate of only 100 kHz by storing the data in analog form until a Level 1 trigger accept.

6.1.1 Switched Capacitor Array Chip

One method of pipelining analog detector signals is through the use of a switched capacitor array (SCA) [23]. This technique provides fast sampling speeds and a wide dynamic range while requiring low cost and low power. Such an approach has been used successfully in the ZEUS experiment [24].

A simplified block diagram of an analog memory cell structure is shown in Figure 6.1. The switched capacitor array chips were originally designed at the Lawrence Berkeley Laboratory [25], and were fabricated by Orbit Semiconductor, Inc., in Sunnyvale, California. The SCA memory consists of 16 parallel channels, each of which has 256 sample-and-hold cells (capacitors). Each sample-and-hold cell consists of a complementary metal oxide semiconductor (CMOS) transmission gate and a 0.7 pF double-polysilicon capacitor. A reference voltage is applied to the bottom plate of each capacitor. The difference between the input signal and the applied reference voltage is therefore the voltage stored on each capacitor.

The SCA chip is addressed externally. The address decoder in the SCA chip uses a break-before-make action, which ensures that an analog signal cannot be split between capacitors. In a given channel, the capacitors can be addressed in any order. Also, a signal can be retrieved from one capacitor while a second signal is being stored in another capacitor, in the same channel, by using separate read and write buses. Thus, the analog pipeline allows for deadtime free operation.

6.1.2 Readout System Design

A schematic diagram of the readout system design is shown in Figure 6.2. The readout system design consists of a dual-range scheme with SCA chips, followed by commercial ADCs. The signals from the calorimeter preamplifiers will be split into two gain scales, and processed by shapers with a greater than 12-bit dynamic range, before being sampled at 40 MHz. This will facilitate the required greater than 15-bit dynamic range. Also, the splitting will reduce the digitization requirements, and thus allow for the use of commercial ADCs. The pulse shaping time is optimized to minimize the effects of noise and pile-up from crossings near in time, but will still

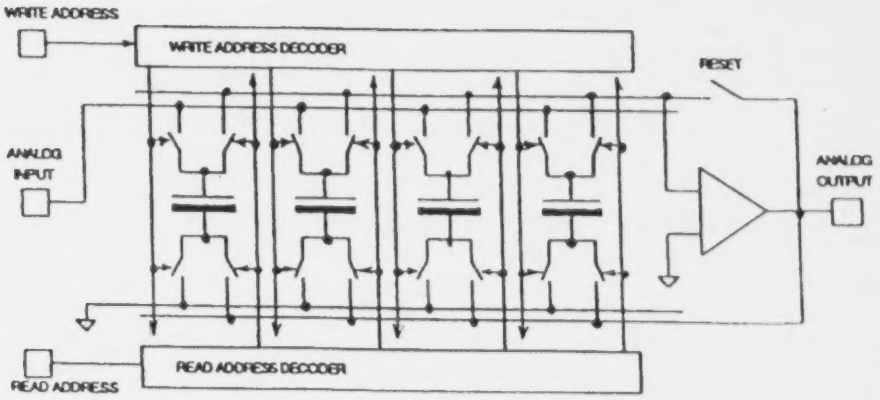

Figure 6.1: A simplified block diagram of an analog memory cell structure (taken from M. Levi *et al.*, "A Switched Capacitor Array Based System for High-Speed Calorimetry", 1991).

preserve the advantages of the calorimeter speed.

There are in fact two types of pile-up. Pile-up in the calorimeter occurs when particles from different collisions pass through the same cells of the calorimeter. This happens because many collisions take place during each bunch-crossing, at essentially the identical time. Pile-up in the calorimeter can not be avoided, but can be reduced by using small calorimeter cells. Pile-up due to the readout electronics is a result of two distinct signals from a calorimeter cell occurring very close to each other in time. In order to minimize this type of pile-up, the calorimeter signals are shaped as quickly as possible.

The stored calorimeter signals are only digitized if the Level 1 trigger accepts them. The digitization time is about 10 μs per sample on average. The high gain signals are compared to the reference voltage before digitization. It is expected that

16 channels will be multiplexed into 12-bit 10 MHz ADCs, and five samples per channel will be digitized. This will reduce the number of ADCs, and hence the cost and power requirements. The SCA addresses and the digital data are then dumped into Level 2 buffers.

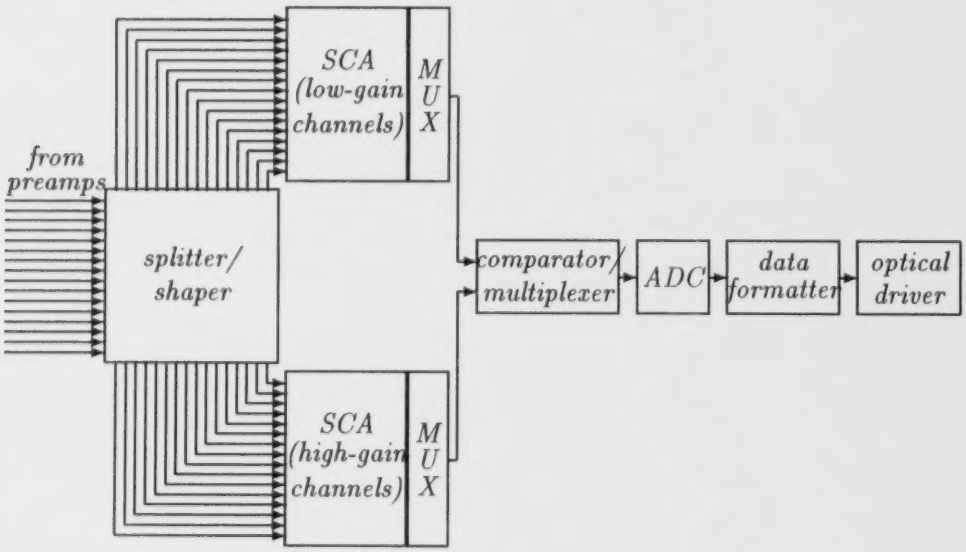

Figure 6.2: Schematic diagram of 16 channels of the readout system design. The timing, control logic, and Level 1 trigger connections are not shown.

Because signals from the electromagnetic calorimeter are formed slowly compared to the bunch-crossing time, it is necessary to readout several calorimeter samples for each Level 1 trigger accept. The number of samples which are read out can be easily changed. Five samples should be sufficient to reconstruct the time and energy

of each signal pulse. Also, the use of five samples should provide adequate discrimination against large pile-up, electronic noise, and signal overlap. It is expected that the required total rms (root mean square) time accuracy will be about 1 ns.

6.2 Pipeline Controller

By allowing simultaneous read and write operations, and the ability to write to non-sequential locations in the SCA, one can obtain deadtime free performance of the pipeline system. Figure 6.3 shows a plot of deadtime versus trigger rate, for different numbers of samples and different readout times. 100 pipeline storage cells per channel are required for a 2.5 μs Level 1 trigger latency and a 40 MHz bunch-crossing frequency. By keeping track of the SCA addresses, one can obtain deadtime free operation provided that the rate of Level 1 accepts does not greatly exceed 100 kHz. Deadtime would occur if data were stored in sequentially located capacitors.

An address list processor (ALP) circuit [26] on the pipeline module is used to control the SCA chip and hence manage the capacitor addresses. The ALP will tag each address as empty, pending Level 1 trigger, or pending readout. In essence, the ALP circuit substitutes movement of analog data (stored signal) for digital data (address of stored signal) [27]. Figure 6.4 shows a block diagram of the address list processor design.

6.3 System Architecture

There are many factors taken into consideration when designing the readout architecture, including: minimizing the amount of electronics on the detector, dividing

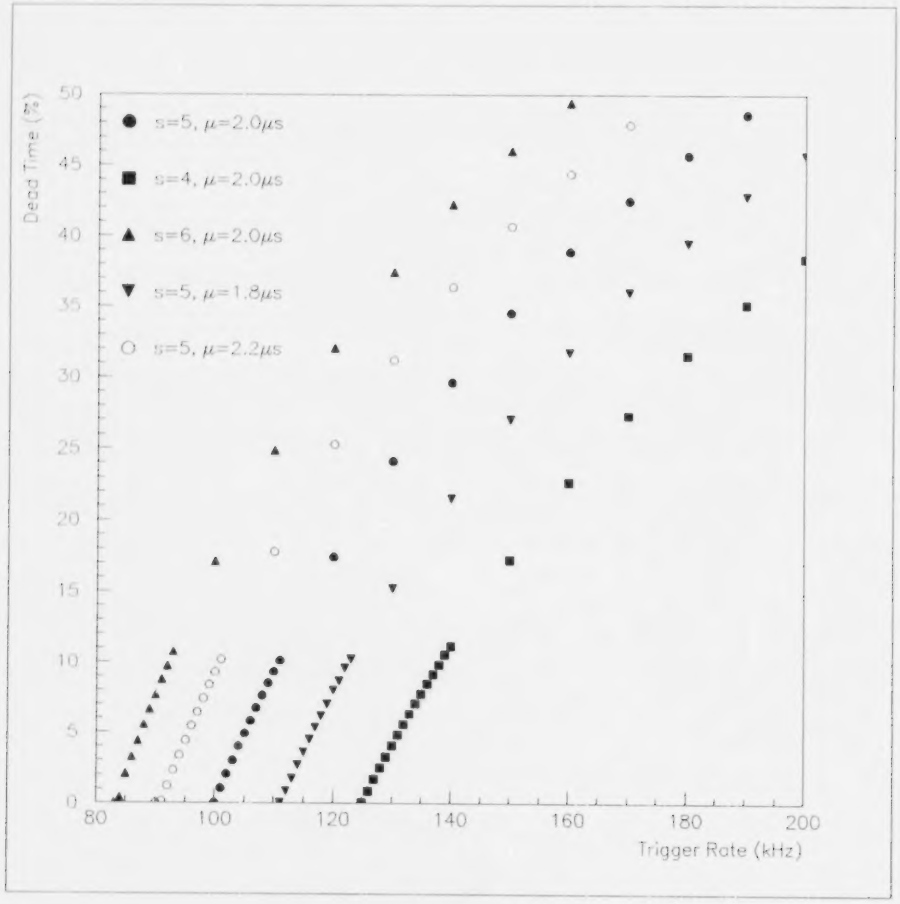

Figure 6.3: Plot of deadtime (as a percentage) versus trigger rate (kHz), for different numbers of samples (s) and different readout times (μ).

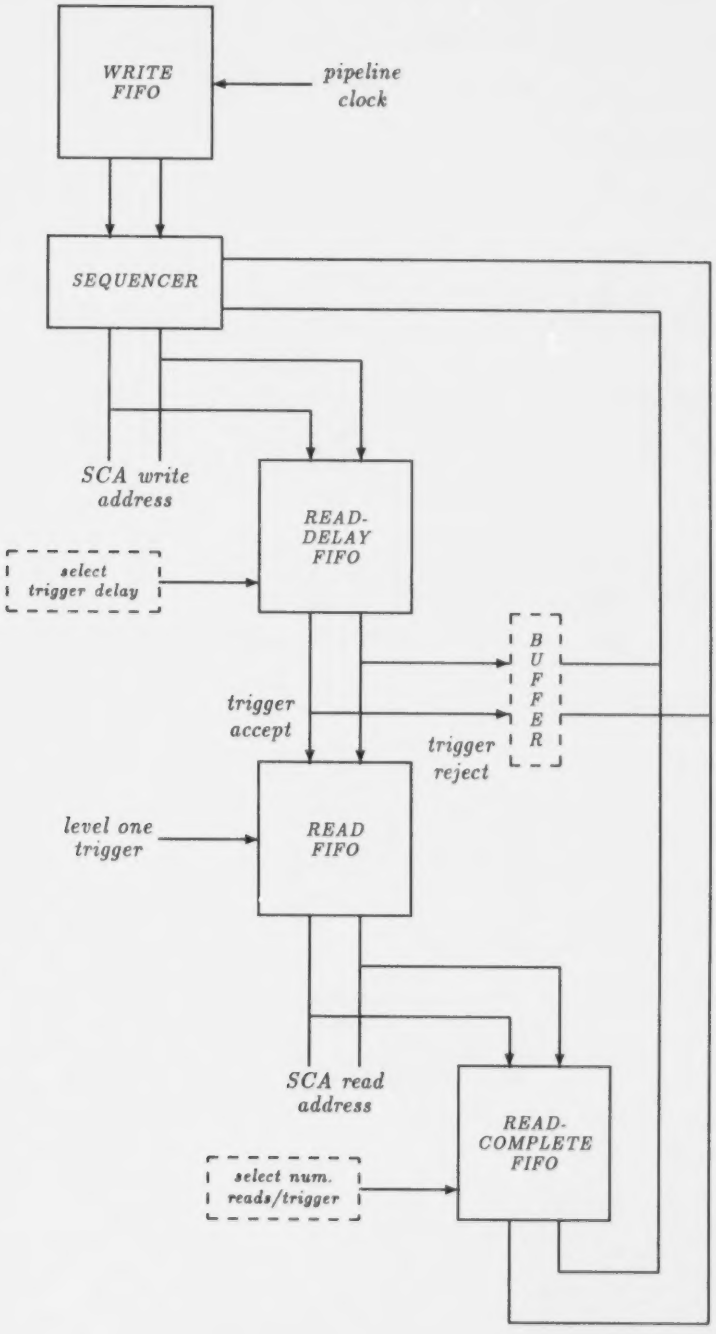

Figure 6.4: Block diagram of the address list processor design.

the system into subsystems, allowing convenient monitoring and calibration, transmitting from the detector only the information for events accepted by the Level 1 trigger, using several samplings for each channel in each selected event, and performing zero-suppression and reconstruction of the energy as soon as possible [27].

The total number of cells which must be read out from the barrel and end-cap electromagnetic calorimeters, the barrel and end-cap hadronic calorimeters, and the forward calorimeters, is roughly 210,000. Thus, the readout electronics will be required to handle 210,000 channels.

The readout electronics will be placed in the gaps between the barrel hadronic calorimeter and the extended barrel hadronic calorimeter. Also, some readout electronics will be located between the extended barrel hadronic calorimeter and the end-cap muon system. The remote electronics could be located in an electronics room a short distance away. It is not acceptable to send shaped analog signals from the detector to an electronics room over long links, due to the large dynamic range.

The basic concepts of the readout architecture are shown in Figure 6.5.

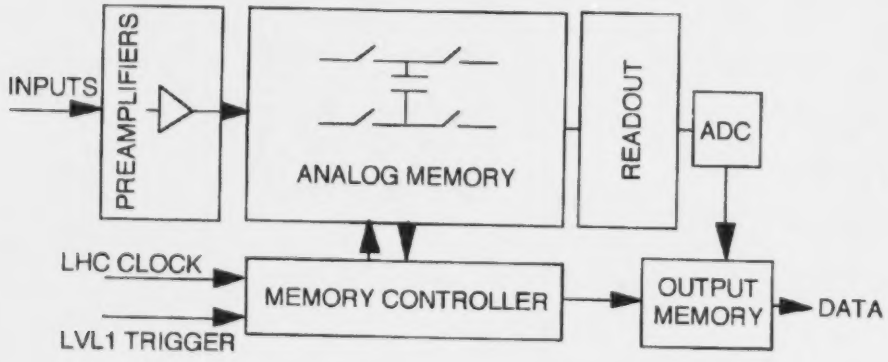

Figure 6.5: Basic concepts of the readout architecture.

6.3.1 Front-End Readout System

The front-end readout electronics will form the Level 1 trigger sums, store the analog signals pending a Level 1 trigger acceptance, and digitize accepted events. Pipeline readout boards will be placed into crates. Each board will be responsible for 64 calorimeter cells. Thus, 3,300 pipeline readout boards are required to read out the 210,000 calorimeter cells. There will be a total of 15 pipeline boards per front-end crate, so 220 crates will be required.

Eight 16-channel SCA chips must be mounted on each pipeline readout board, because each board is responsible for 64 calorimeter cells (128 shaper channels). This will require eight 12-bit 10 MHz ADCs per board. Figure 6.6 shows the layout of the pipeline readout boards.

Each board will have one local pipeline controller. The ALP circuit will provide the write and read addresses to all the SCA chips on the board. The ATLAS timing, trigger and control distribution system [28] will provide the 40 MHz LHC clock, the Level 1 trigger decision, the event number, and the trigger type to each controller. The crate pipeline controller will then transmit the set of fast timing signals to the analog pipeline boards. The timing of these signals must be accurate to 0.5 ns with respect to the LHC bunch-crossing time.

A calibration board in each front-end crate will control the calibration system for that crate. The calibration system must be able to inject calibration pulses with a programmable amplitude and time of arrival. The charge injection must be able to exercise the full dynamic range of the readout [27].

In total, each front-end crate will contain 15 pipeline readout boards, one trigger summation board, one local pipeline controller, and one calibration controller.

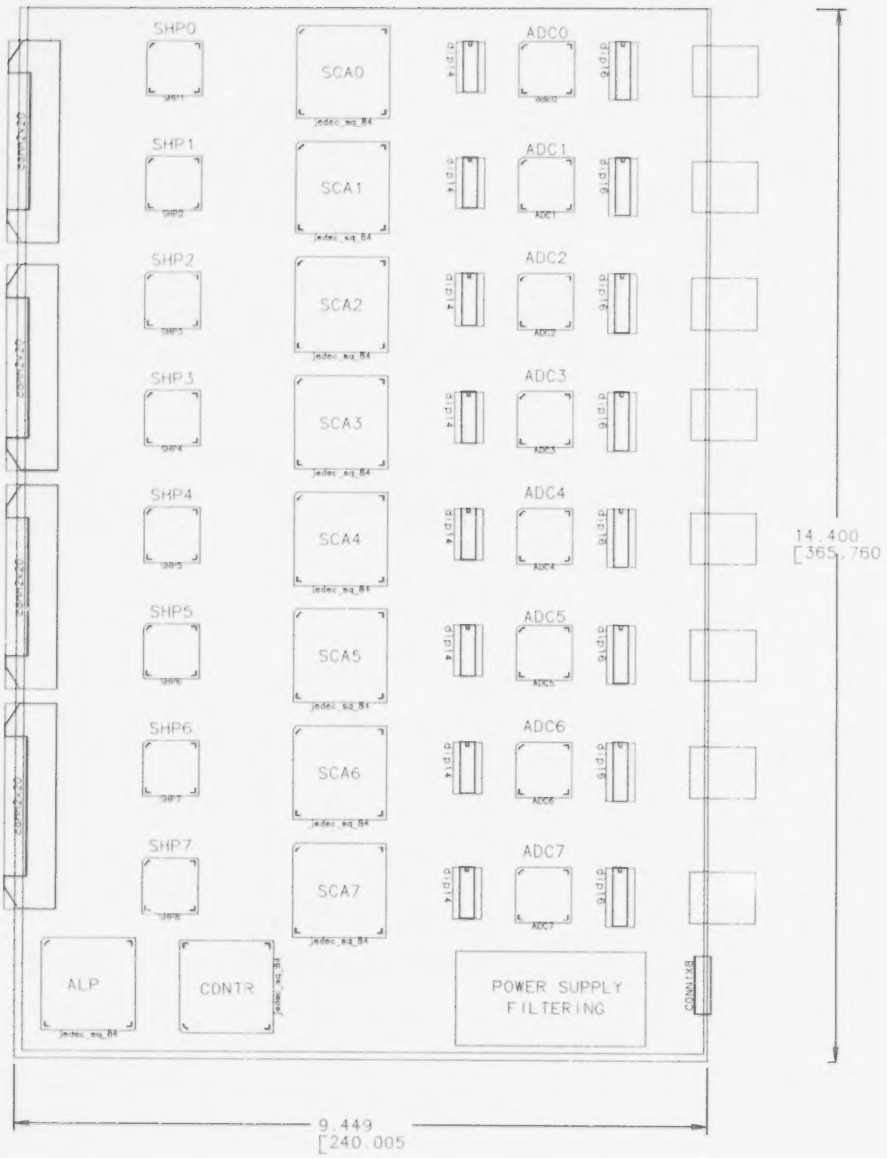

Figure 6.6: Layout of the pipeline readout boards.

6.3.2 Remote Electronics

The remote electronics is responsible for processing the digital signals, and interfaces to the Level 2 trigger and data acquisition systems. Each digital processing board will receive synchronous signals at 10 MHz over 32 optical fibres from eight pipeline readout boards. The digital processing boards will have the required number of CPUs to perform pulse reconstruction and data formatting. The results will then be made available to the Level 2 trigger and data acquisition systems. A total of 250 digital processing boards located in 21 VME crates (12 boards per crate) will be required for the remote electronics.

6.4 Previous Test Results

A prototype readout system was used for tests with the RD3 liquid argon accordion calorimeter [17] at the SPS (Super Proton Synchrotron) at CERN. The main objective was to readout real calorimeter signals with a 12-bit resolution.

The tests were carried out in September of 1993 [27]. For a full scale voltage range of 2.5 V, the average rms variation in the pedestal[1] for each capacitor was measured to be about 1.2 mV. The noise per capacitor was determined to be 0.73 mV incoherent over the channels, and 0.31 mV coherent over the channels. Over the capacitors in any single channel, a negligible coherent noise was observed. After circuit-board improvements, the rms noise per capacitor was determined to be (0.610 ± 0.006) mV, where the error is statistical only. It is estimated that approximately 0.2 mV rms noise is due to the ADC alone and 0.5 mV rms noise is due to the system without the SCA chip.

[1]The pedestal value is the output when there is no applied input; *ie.* the "zero" of a cell.

In order to achieve a 12-bit dynamic range, the pedestal variation of each of the storage capacitors in a channel must be less than one part in $2^{12} = 4096$ of the full scale voltage range. Thus, a channel operating with the full scale range of 2.5 V would require about 0.61 mV of pedestal variation per capacitor. The above results indicate that the resolution of the system was 11-12 bit. A 12-bit resolution could be obtained by storing the pedestal value for each capacitor in the system, rather than having one pedestal value per channel.

6.5 Present Work

This thesis focuses on two types of tests that have been performed on the SCA chip during the past two years. The electronic noise of all of the components of the readout system must be determined, and so the noise of the SCA chip has been studied. The rms noise of the chip has been measured, and the contributions to the noise have been analyzed. Another interesting test that has been performed on the SCA chip is a study of the chip's response to radiation. SCA chips were exposed to radiation in the form of electrons, protons and photons, and the performance of the chips was recorded in each case.

Chapter 7 of this thesis presents the results of the noise analysis tests that were performed on SCA chips. Chapter 8 documents the sensitivity and response of the SCA chips to radiation. Table 6.1 contains information about each of the tests.

In September of 1995, a prototype readout system was tested at CERN, using the RD3 calorimeter. The test data are currently being analyzed, and more testing will be performed at CERN in 1996.

Date Data were Taken	*Location of Testing*	*Tests Performed*
September 1994	CSR, UofA	Noise Analysis; Addressing Test
October 1994	CSR, UofA	Stray Capacitance Test; Analysis of Individual Capacitors
November 1994	CSR, UofA	Capacitor Uniformity Check; Voltage Drift Test
September 1993	CERN, Geneva	Noise Analysis of RD3 Calorimeter Data
June-July 1994	CERN, Geneva	Exposure to Electron and Proton Radiation
July-December 1995	Department of Chemistry, UofA	Exposure to Gamma Radiation

Table 6.1: The tests which have been performed on SCA chips. (CSR, UofA denotes the Centre for Subatomic Research, University of Alberta.)

CHAPTER 7

Noise Analysis

In order to obtain a large dynamic range, it is essential that the noise of the electronics be minimized. Tests were performed to determine the rms noise of the SCA chips. Two pedestal and two voltage runs were performed[1] in the summer of 1994. Two chips were used, with each chip tested both with an arbitrary voltage at the input, and with no voltage applied (pedestal). The chips used were at room temperature (no heating or cooling was done to the chips). Four of the 16 SCA channels in each chip were repeatedly read out. The full scale during these tests was 4096 ADC counts (12-bit). Table 7.1 shows the number of events in each run.

Run # and type	*Number of events*
Run 1 - Volts	638,099
Run 2 - Pedestal	552,534
Run 3 - Volts	461,089
Run 4 - Pedestal	352,778

Table 7.1: Number of events in each run.

The total noise (rms variation) is taken to be a combination of two noise components. There is a coherent noise, which affects all of the channels simultaneously and is due to common electronics in the system. And there is an incoherent noise

[1]The tests were performed by Lars Holm, senior technician, Centre for Subatomic Research, University of Alberta.

which is completely random. These two noise components add in quadrature to give the total noise,

$$\rho^2_{total} = \rho^2_{incoh} + \rho^2_{coh}.$$

The coherent noise was not measured, but rather was estimated mathematically[2]. Let x_{ijk} be the measured value (in ADC counts) of capacitor i in channel j for event k. First, the mean ADC counts μ_{ij} for each cell (capacitor i, channel j) were calculated. Then, for each event k, where there are N events in total, the deviations from the means were determined for each of the p channels:

$$A_{i0k} = x_{i0k} - \mu_{i0},$$

$$A_{i1k} = x_{i1k} - \mu_{i1},$$

$$A_{i2k} = x_{i2k} - \mu_{i2},$$

$$A_{i3k} = x_{i3k} - \mu_{i3},$$

$$\vdots$$

$$A_{i(p-1)k} = x_{i(p-1)k} - \mu_{i(p-1)},$$

where i (capacitor address) is fixed for a given k (event). Then, a sum (S^+_k) and an alternate sum (S^-_k) were determined for each event k:

$$S^+_k = A_{i0k} + A_{i1k} + A_{i2k} + A_{i3k} + \cdots + A_{i(p-1)k},$$

$$S^-_k = A_{i0k} - A_{i1k} + A_{i2k} - A_{i3k} + \cdots - A_{i(p-1)k}.$$

[2]Method developed by Dr. D.M. Gingrich.

At this point, it can be seen that if the noise is totally random, then S_k^+ and S_k^- would be approximately the same. However, if the noise has a coherent component that causes all of the channels to shift at once, then S_k^+ would be greater than S_k^-, because the alternate sum would force the coherent parts to cancel out. This is the key to the method.

Next, the errors σ_+^2 and σ_-^2 on the two sums S_k^+ and S_k^- were estimated using:

$$\sigma_+^2 = \frac{1}{N-1}\sum(S_k^+)^2,$$

$$\sigma_-^2 = \frac{1}{N-1}\sum(S_k^-)^2,$$

where the summation is over events k.

The coherent noise σ_{coh} across the p channels was then estimated as:

$$\sigma_{coh} = \frac{\sqrt{\sigma_+^2+\sigma_-^2}}{p}.$$

(Please see Appendix A for a derivation).

This approximation could be improved if a larger number of channels were used (four channels were used in the test), but is nonetheless considered to be fairly good in this case due to the large number of events.

The total noise of the system is calculated as the usual rms variation. Once the coherent noise has been estimated using the above method, the incoherent noise can be determined, since the two noise components add in quadrature.

The results are shown in Table 7.2. The tails of the ADC distributions were excluded, using cuts of various sizes. The total noise, coherent noise and incoherent

Cut Size = ± 41 adc	*Total Noise*	*Coherent*	*Incoherent*	*% Cut*
Run 1 - Volts	1.421	0.976	1.033	0.855
Run 2 - Pedestal	1.757	1.419	1.036	0.446
Run 3 - Volts	1.566	1.166	1.045	0.866
Run 4 - Pedestal	1.987	1.677	1.066	0.434
Cut Size = ± 20 adc	*Total Noise*	*Coherent*	*Incoherent*	*% Cut*
Run 1 - Volts	1.419	0.974	1.033	0.856
Run 2 - Pedestal	1.735	1.409	1.012	0.462
Run 3 - Volts	1.563	1.163	1.045	0.868
Run 4 - Pedestal	1.951	1.668	1.011	0.462
Cut Size = ± 8 adc	*Total Noise*	*Coherent*	*Incoherent*	*% Cut*
Run 1 - Volts	1.417	0.970	1.033	0.871
Run 2 - Pedestal	1.707	1.376	1.010	0.711
Run 3 - Volts	1.558	1.156	1.045	0.909
Run 4 - Pedestal	1.907	1.619	1.008	0.890

Table 7.2: Results of noise analysis tests.

noise values are shown in ADC counts for all four channels, for the various cuts. Also, the percentage of data excluded by the cuts is shown in each case.

So it appears that the incoherent noise of the SCA chip is about 1 ADC count. The coherent noise ranged from 1.0 to 1.7 ADC counts. The significance of the total noise of the system being about 1.4 to 2.0 ADC counts is that if the dynamic range of the system were for example 12-bit, the noise of the system would degrade the effective resolution to about 11-bit.

7.1 Addressing Test

It was thought that the coherent noise may have been due to the addressing of the SCA chip. To test this, a plot of total noise versus capacitor address was made. From this, it was determined which capacitors were the most noisy. In general, the noisiest capacitors were those which have a large number of bits set compared to the previous address. The 18 most noisy capacitors were then excluded from the coherent/incoherent noise analysis.

The results of the noise analysis, with the 18 most noisy capacitors excluded, are shown in Table 7.3. If the coherent noise decreased but the random (incoherent) noise remained the same, then one would conclude that the coherent noise is due to the addressing. Comparing Table 7.2 with Table 7.3, one can see that both the coherent noise and incoherent noise decreased when the 18 most noisy capacitors were excluded. Although the coherent noise decreased more than the incoherent noise, it was concluded that the addressing was not responsible for the coherent noise.

7.2 Stray Capacitance and Bus Reset Tests

It is possible that a signal passing through the SCA chip could affect the next signal. Any residual charge from the first signal would falsely inflate the magnitude of the second signal, when it is stored in the chip. This could cause significant errors in the values that would be obtained in any experiment.

Tests were performed to determine if there was any residual charge in the SCA chip after a relatively high voltage signal is read. In order to study this, three runs were performed[3]. Two channels of a SCA chip were used. In the first run, only pedestal values were read out. In the second run, the SCA chip was under voltage. The third run alternated between voltage applied and no voltage applied. The full scale in these tests was 16384 ADC counts (14-bit).

Table 7.4 shows the number of events in each run. In Run 3, approximately half of the events are pedestal values, and the other half are voltage values.

The data from Run 3 were split into the pedestal and voltage components. This was done so that the pedestal and voltage components could be compared to Runs 1 and 2, respectively. Thus, there were a total of four different data samples. Also, the values for the voltage readings are actually pedestal-subtracted voltages. This is necessary to be able to interpret the voltage values correctly, because each capacitor will have a different pedestal value.

For each run, the mean number of ADC counts and the rms variation were calculated for each of the two channels. In all three runs, there were a number of data points which were clearly separated from the main distributions. These outliers were not used in the analysis, in order to study only the main distributions. In Run 1,

[3]The tests were performed by Lars Holm, senior technician, Centre for Subatomic Research, University of Alberta.

Cut Size = ± 41 adc	*Total Noise*	*Coherent*	*Incoherent*	*% Cut*
Run 1 - Volts	1.386	0.932	1.026	0.855
Run 2 - Pedestal	1.689	1.347	1.019	0.450
Run 3 - Volts	1.528	1.123	1.036	0.865
Run 4 - Pedestal	1.915	1.598	1.054	0.432
Cut Size = ± 8 adc	*Total Noise*	*Coherent*	*Incoherent*	*% Cut*
Run 1 - Volts	1.382	0.926	1.026	0.861
Run 2 - Pedestal	1.657	1.321	1.000	0.597
Run 3 - Volts	1.522	1.115	1.036	0.885
Run 4 - Pedestal	1.859	1.567	1.001	0.710

Table 7.3: Results of noise analysis tests, with the 18 noisiest capacitor addresses excluded.

Run # and type	*Number of events*
Run 1 - Pedestal	410,210
Run 2 - Voltage	423,247
Run 3 - Ped./Volt.	439,736

Table 7.4: Number of events for each run in the stray capacitance test.

approximately 1,800 events were at least 500 ADC counts above the mean pedestal values, and so were excluded from the calculations. In Run 2, about 4,000 events differed from the mean values by more than 200 ADC counts, and were excluded from the calculations. In Run 3, approximately 20,000 events differed by at least 200 ADC counts from the pedestal and voltage means, and were excluded. The mean number of ADC counts and the rms variation for both channels and all three runs is shown in Table 7.5.

	Run 1 - Ped.		*Run 2 - Volts*		*Run 3 - Ped.*		*Run 3 - Volts*	
	Mean	RMS	Mean	RMS	Mean	RMS	Mean	RMS
Ch. 0	1670	39.7	12100	39.7	1714	48.9	12040	49.6
Ch. 1	1614	51.6	12080	41.9	1652	64.0	12000	49.3

Table 7.5: Number of ADC counts and rms variation for both channels and all three runs in the stray capacitance test.

It was determined that the pedestal values increased by about 40 ADC counts when the input signal alternated between pedestal and high voltage. Also, the voltage values decreased by about 70 ADC counts for the same run. The noise increased in both cases. Thus, it appears that the SCA chip is susceptible to stray capacitance. However, the data were much noisier than expected, as compared to previous tests, which made it very difficult to draw conclusions from this test. Also, the events that were considered to be outliers and were excluded from the calculations would cause a larger shift in the means and a much greater noise if they were included.

7.2.1 Individual Capacitors

It appeared that a study of the behavior of individual capacitors during the test may be worthwhile. To this end, the data for individual capacitors were examined. Sixteen capacitors, selected at random, were studied. The same eight capacitor addresses were used for both channels. For each capacitor, four different samples were available: the pedestal values from Run 1, the voltage values from Run 2, the pedestal values from Run 3, and the voltage values from Run 3. The amount of data obtained for each capacitor is shown in Table 7.6.

For each of the sixteen capacitors, the mean number of ADC counts and the rms deviation were calculated for each run. In Run 1, the value for one of the events was at least 600 ADC counts above the mean value, and so was excluded from the calculations. In Run 2, at most five events for each capacitor differed from the mean values by at least 50 ADC counts, and so were omitted from the calculations. In Run 3, for each capacitor, at most 75 events differed from the mean values by at least 50 ADC counts, and were also excluded from the calculations. These values that differ from the means are significant, but are clearly separated from the main peaks around the means. The mean number of ADC counts and the rms variation for each capacitor are shown in Tables 7.7 and 7.8 for Channels 0 and 1 respectively.

For the individual capacitors, it was determined that when the input signal alternated between pedestal and voltage, the pedestal values were about 50 ADC counts greater than before, and the voltage values were about 70 ADC counts lower than before. Also, the RMS noise increased. Thus, it was concluded that all of the capacitors studied were affected by stray capacitance.

Cap. #	*Channel*	*Run 1 Ped.*	*Run 2 Volts*	*Run 3 Ped.*	*Run 3 Volts*
0	0	1514	1642	931	788
	1	1514	1642	931	788
12	0	1625	1693	899	833
	1	1625	1693	899	833
25	0	1613	1689	936	837
	1	1613	1689	936	837
143	0	1488	1620	913	855
	1	1488	1620	913	855
187	0	1630	1697	912	852
	1	1630	1697	912	852
204	0	1560	1660	870	838
	1	1560	1660	870	838
240	0	1595	1720	919	822
	1	1595	1720	919	822
255	0	1545	1683	914	870
	1	1545	1683	914	870

Table 7.6: Number of events obtained for each capacitor.

Cap.	*Run 1 - Ped.*		*Run 2 - Volts*		*Run 3 - Ped.*		*Run 3 - Volts*	
#	Mean	RMS	Mean	RMS	Mean	RMS	Mean	RMS
0	1681	3.51	12100	2.95	1740	4.92	12000	4.78
12	1627	4.36	12150	1.78	1660	6.50	12100	4.19
25	1590	5.05	12190	2.34	1626	4.39	12140	4.83
143	1653	3.59	12110	2.47	1702	5.17	12040	4.23
187	1684	3.80	12080	1.79	1738	5.03	12010	5.44
204	1723	3.66	12060	1.45	1781	4.73	11990	5.42
240	1760	3.81	12000	1.26	1822	4.08	11920	5.02
255	1653	3.68	12150	2.91	1714	6.56	12080	4.26

Table 7.7: Mean number of ADC counts and rms variation for Channel 0 - all three runs.

Cap.	*Run 1 - Ped.*		*Run 2 - Volts*		*Run 3 - Ped.*		*Run 3 - Volts*	
#	Mean	RMS	Mean	RMS	Mean	RMS	Mean	RMS
0	1606	3.56	12070	2.53	1653	5.24	11970	4.59
12	1553	3.99	12130	1.49	1589	8.36	12070	5.75
25	1520	4.97	12160	1.83	1556	7.88	12100	5.45
143	1590	4.17	12080	2.23	1632	7.03	12010	5.14
187	1634	4.08	12050	1.62	1687	5.75	11980	4.99
204	1682	3.93	12030	1.33	1738	4.99	11960	5.40
240	1730	3.97	11970	1.91	1790	4.48	11890	4.75
255	1570	3.81	12100	2.19	1623	6.95	12020	4.59

Table 7.8: Mean number of ADC counts and rms variation for Channel 1 - all three runs.

7.3 Board Modification

The readout board was changed so that the capacitors were addressed sequentially, in an attempt to reduce the noise, and new data were obtained. Two runs were performed[4], using one SCA chip. Each run used two channels and consisted of about 500,000 events. Again, the tests were performed using a 14-bit ADC. In the first run, only pedestal values were read out. In the second run, the chip was under voltage. It is of interest to determine whether the new voltage and pedestal data are less noisy than the original data.

Table 7.9 shows the mean number of ADC counts and the rms variation for the new pedestal and voltage runs, and also shows the pedestal-subtracted voltage values.

	Run 1 : Ped.		*Run 2 : Volts*		*Volts - Ped.*	
	Mean	RMS	Mean	RMS	Mean	RMS
Ch. 0	1678	9.7	7757	7.0	6079	5.6
Ch. 1	1619	7.3	7690	5.9	6072	7.4

Table 7.9: Mean number of ADC counts and rms variation for both channels.

Histograms of the pedestal-subtracted voltage data for both channels are shown in Figure 7.1.

The results of the modifications to the readout board are very encouraging. The outliers that appeared in the original data have completely disappeared in the new data. Also, by comparing Table 7.9 with Table 7.5, one can see that the rms

[4]The tests were performed by Lars Holm, senior technician, Centre for Subatomic Research, University of Alberta.

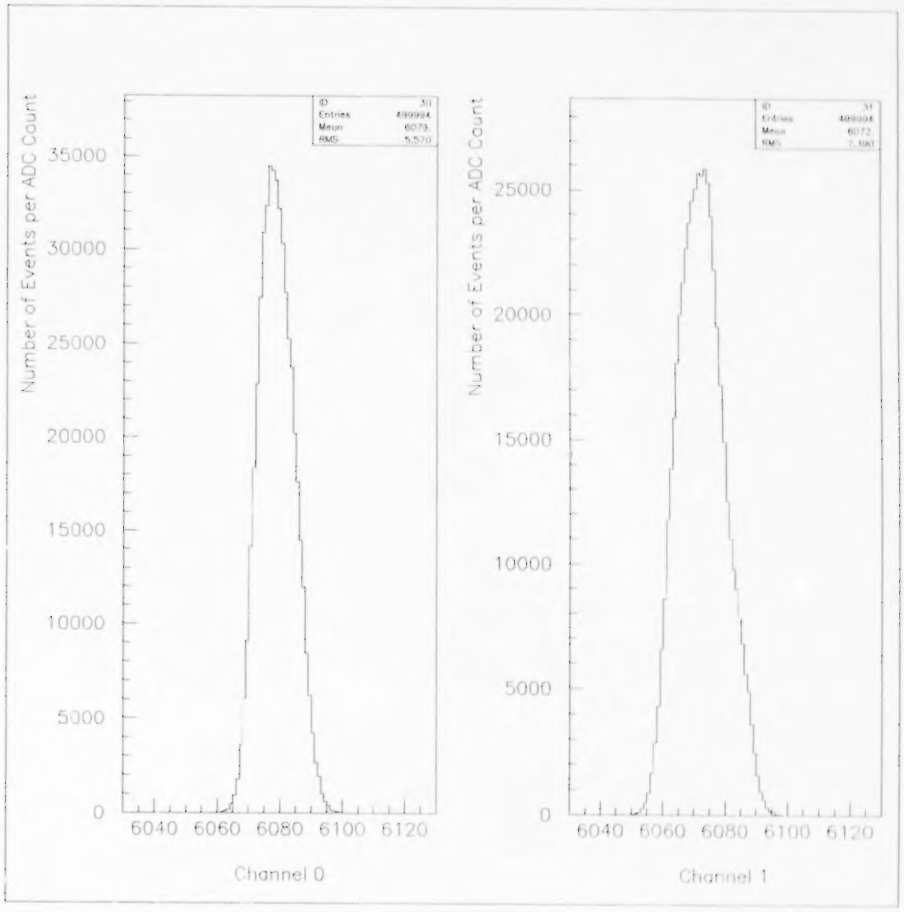

Figure 7.1: Histograms of ADC counts for pedestal-subtracted voltage data (both channels.

noise has decreased considerably in the new data, although it is still somewhat greater than expected, based on the results of SCA tests performed in the summer of 1994.

7.3.1 Capacitor Uniformity Check

The plots of pedestal-subtracted voltage ADC counts in Figure 7.1 are non-Gaussian, and are somewhat oddly shaped. In order to determine the reason for the non-Gaussian distribution, the mean ADC counts of individual capacitors were studied. The same data were used as above; one pedestal run and one voltage run were studied, with two channels used in each case. There is a total of 256 capacitors in each channel. Plots of mean ADC counts versus capacitor address for both channels and for pedestal, voltage and pedestal-subtracted voltage data are shown in Figures 7.2 and 7.3.

Figures 7.2 and 7.3 show very interesting trends. In Channel 0, the mean voltage values increased slightly with increasing capacitor address, and the mean pedestal values increased at a greater rate with increasing capacitor address. Consequently, the mean pedestal-subtracted voltage values decreased with increasing capacitor address for Channel 0. In Channel 1, the mean voltage values were roughly constant for all capacitor addresses, but the mean pedestal values increased with increasing capacitor address. Thus, the mean pedestal-subtracted voltage values decreased with increasing capacitor address. The fact that the mean pedestal-subtracted voltage values were not constant across the capacitors in each channel led to the unexpected shapes of the distributions in Figure 7.1. It can be seen in Figures 7.2 and 7.3 that in both Channels 0 and 1, the mean pedestal-subtracted values decreased across the capacitors by about 15 ADC counts. Furthermore, in Channel 1, the mean pedestal-subtracted voltage values seemed to alternate from one capacitor to the next between a high and a low mean. The difference between the two means is about 8 ADC counts.

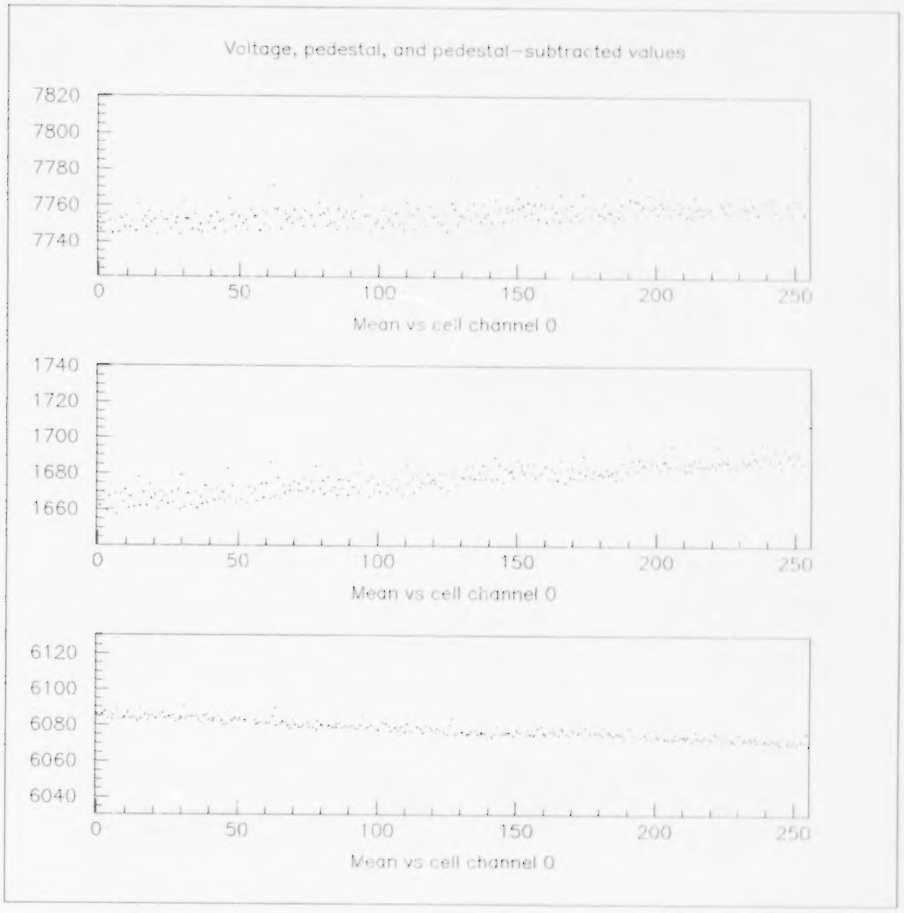

Figure 7.2: Mean ADC counts versus capacitor address for Channel 0.

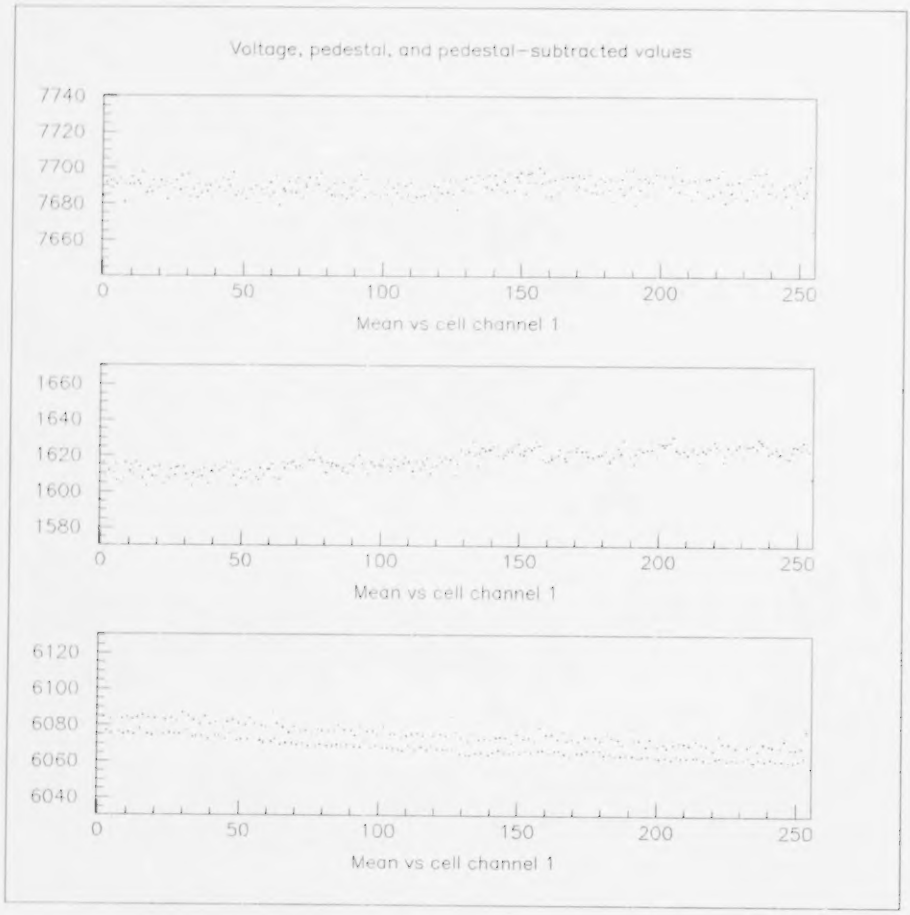

Figure 7.3: Mean ADC counts versus capacitor address for Channel 1.

7.3.2 Voltage Drifting

The new data were analyzed to determine if there is any time-dependent variation due to voltage drifting. In order to check this, the pedestal, voltage and pedestal-subtracted voltage data were each separated into two halves - the first half and the second half. Then, a plot of ADC counts was made for each half, and the results from both halves were compared to determine if the mean ADC counts and/or RMS changed from the first half of a run to the second half. The results of this test were that the mean number of ADC counts was identical in the first and second halves of each run, and the RMS values changed only slightly (about 2%). Thus, it was concluded that there was no voltage drift in the data. This is encouraging, because any time-dependent variation in the voltage would cause significant uncertainty in an experiment.

7.3.3 Summary

The SCA chip studied was susceptible to stray capacitance. It is desirable to remedy this in future design modifications. Also, pedestal-subtracted voltage values were not uniform across a given channel, and in fact a ramp across channels was observed. No drift in voltage over time was observed for the SCA chip.

7.4 Analysis of the Coherent and Incoherent Noise Components of the RD3 Calorimeter Data

In September of 1993, a readout system based on switched capacitor array chips was tested using the RD3 calorimeter. An analysis of the tests [29] was performed by the

High Energy Physics group at the University of Alberta. This chapter describes a detailed analysis of the electronic noise during the pedestal runs. Details of the RD3 calorimeter have been described elsewhere [30].

7.4.1 Introduction

As mentioned earlier, in order to minimize the electronic noise of the readout system, it is crucial to understand the source and magnitude of the various contributions to the noise. This is the motivation behind the noise analysis of the RD3 data.

During the RD3 calorimeter testing, the readout system consisted of five readout modules and a controller board. Each readout module contained two SCA chips with 16 channels each. Only 12 of the 16 channels in each SCA chip were used, to simplify the connections to the shaper electronics. Thus, a total of 120 channels were used. The signals were digitized by 12-bit ADCs, so the full scale is 4096 ADC counts.

7.4.2 Pedestal Data

Noise analysis has been performed on five pedestal runs. Table 7.10 shows the number of events in each of the five corresponding data files.

The number of ADC counts ranged from about 30 to 200 counts. The mean pedestal value in each of the 14 pedestal runs lay between 91 and 95 ADC counts. A total of ten time samples, numbered 0 - 9, were read out for each event.

It was observed that Channels 72 and 73 were dead, and so they have been excluded from all analysis. Thus, the total number of channels studied is 118. Also, Capacitor 170 in Channels 48 to 59 has been excluded because it is about 70 ADC

counts above average. Furthermore, the first (0) and last (9) time samples were observed to be significantly different from the others, and thus have been excluded from the analysis. However, no time sample corrections were employed.

7.4.3 Coherent and Incoherent Noise

The total noise of the system is calculated as the usual rms variation. The coherent noise has been estimated using the method detailed earlier in this chapter. The coherent noise is then easily calculated, because the two noise components add in quadrature ($\rho^2_{total} = \rho^2_{incoh} + \rho^2_{coh}$).

Noise analysis (*ie.* determination of the noise components) was performed separately for the entire system, for individual boards (modules), and for individual chips.

7.4.4 Entire System Analysis

The coherent noise across all 118 channels in the system was approximated for each of the five pedestal data files, treating the different time samples separately. Outliers and/or tails of the ADC distributions were excluded, using a cut of size $\pm$ 20 ADC counts. The amount of data excluded by this cut ranged from 0 to 10.5%.

Table 7.11 shows the total noise, coherent noise, and incoherent noise for each run, averaged over the eight time samples.

Table 7.12 shows the total noise, coherent noise, and incoherent noise for each time sample, averaged over the five runs.

Table 7.13 shows the global averages for the total, coherent and incoherent

Run	*Number of events*
Run 1 - la0716.seq4	919
Run 2 - la0719.seq7	2689
Run 3 - la0731.seq2	2654
Run 4 - la0731.seq5	875
Run 5 - la0739.seq4	2608

Table 7.10: Number of events in each of the five pedestal runs studied.

Run	*Total Noise*	*Coherent*	*Incoherent*
Run 1 - la0716.seq4	1.27	0.30	1.23
Run 2 - la0719.seq7	1.31	0.33	1.26
Run 3 - la0731.seq2	1.30	0.34	1.26
Run 4 - la0731.seq5	1.28	0.34	1.23
Run 5 - la0739.seq4	1.30	0.34	1.25

Table 7.11: Noise values for each run, averaged over time samples.

noise.

The total noise of the system during the pedestal tests is about 1.3 ADC counts. The coherent noise of the system was estimated to be about 0.33 ADC counts. The noise of the SCA chip (the incoherent noise) is calculated to be about 1.2 to 1.3 ADC counts. The coherent noise is small enough relative to the incoherent noise that the noise of the SCA chip is only slightly less than the total noise of the system.

Runs 2, 3 and 5 were slightly noisier than Runs 1 and 4. It is interesting to note that Runs 2, 3 and 5 had over 2600 events each, while Runs 1 and 4 only had about 900 events each.

Prior to making a cut, the later time samples were much noisier than the earlier ones. After the cut of $\pm$ 20 ADC counts was made, the time samples had similar noise values, although the later time samples were still slightly noisier.

It has been estimated that there is a noise contribution from the preamplifiers and shaping amplifiers of about 0.6 ADC counts, incoherent over the channels [29]. Taking this into consideration, since the average noise per capacitor is about 1.3 ADC counts, the average noise in the pipeline system is thus between 1.1 and 1.2 ADC counts. Using the estimated coherent noise of about 0.3 ADC counts, the incoherent noise of the pipeline system is thus calculated to be about 1.1 ADC counts. However, when considering these values, it is important to note that the ADC is only accurate to $\pm$ 0.5 ADC counts.

Time Sample	*Total Noise*	*Coherent*	*Incoherent*
1	1.29	0.31	1.25
2	1.28	0.30	1.24
3	1.27	0.29	1.24
4	1.27	0.30	1.24
5	1.28	0.32	1.24
6	1.30	0.34	1.26
7	1.31	0.37	1.25
8	1.32	0.42	1.26

Table 7.12: Noise values for each time sample, averaged over runs.

Total Noise	*Coherent*	*Incoherent*
1.29	0.33	1.25

Table 7.13: Global pedestal noise values, averaged over the eight time samples and five runs.

7.4.5 Board Analysis

The coherent noise across the 24 channels in each of the five boards was approximated for two of the pedestal data files - la0716.seq4 (Run 1) and la0719.seq7 (Run 2). Again, the values were calculated for all eight time samples. (Note: Board 4 only contained 22 channels, numbered 74 - 95, because Channels 72 and 73 were dead.) Outliers and/or tails of the ADC distributions were excluded, using a cut of $\pm$ 20 ADC counts. The amount of data excluded by this cut ranged from 0 to 10.1%. Most of the data that were cut existed in the last three time samples.

Table 7.14 shows the noise values averaged over time samples for each of the five boards in Run 1.

Board	*Channels*	*Total Noise*	*Coherent*	*Incoherent*
1	0 - 23	1.25	0.46	1.16
2	24 - 47	1.26	0.39	1.20
3	48 - 71	1.19	0.34	1.14
4	74 - 95	1.30	0.43	1.22
5	96 - 119	1.45	0.63	1.31

Table 7.14: Averages across time samples for Run 1 - la0716.seq4.

Table 7.15 shows the noise values averaged over time samples for each of the five boards in Run 2.

The total noise of each of the five boards during the pedestal tests ranged from 1.2 to 1.5 ADC counts. The coherent noise ranged from 0.34 to 0.67 ADC counts. The incoherent noise ranged from 1.1 to 1.3 ADC counts.

Board 3 had the least coherent noise, averaged over time samples. In Run 1,

Board 3 had a coherent noise of 0.34 ADC counts, and in Run 2, Board 3 had a coherent noise of 0.37 ADC counts. Board 5 had the most coherent noise, averaged over time samples. In Run 1, Board 5 had a coherent noise of 0.63 ADC counts. In Run 2, Board 5 had a coherent noise of 0.67 ADC counts.

The average total noise of each board in Run 1 is 1.3 ADC counts. The average coherent and incoherent noise of each board in Run 1 is 0.45 ADC counts and 1.2 ADC counts respectively. For Run 2, the average total noise, coherent noise and incoherent noise values are 1.3 ADC counts, 0.48 ADC counts and 1.2 ADC counts respectively.

The total, coherent and incoherent noise in Run 2 was greater than Run 1 for all five boards.

7.4.6 Chip Analysis

The coherent noise across the 12 channels for each of the ten SCA chips was approximated for two of the pedestal data files - la0716.seq4 (Run 1) and la0719.seq7 (Run 2). Again, the values were calculated for all eight time samples. (Note: Chip 7 only contained 10 channels, numbered 74 - 83, because Channels 72 and 73 were dead.) Outliers and/or tails of the ADC distributions were excluded, using a cut of $\pm$ 20 ADC counts. The amount of data excluded by this cut ranged from 0 to 9.7%. Most of the data that were cut existed in the last three time samples.

Table 7.16 shows the noise values averaged over time samples for each of the ten chips in Run 1.

Table 7.17 shows the noise values averaged over time samples for each of the ten chips in Run 2.

Board	*Channels*	*Total Noise*	*Coherent*	*Incoherent*
1	0 - 23	1.29	0.47	1.20
2	24 - 47	1.32	0.42	1.25
3	48 - 71	1.22	0.37	1.16
4	74 - 95	1.34	0.48	1.25
5	96 - 119	1.49	0.67	1.32

Table 7.15: Averages across time samples for Run 2 - la0719.seq7.

Chip	*Channels*	*Total Noise*	*Coherent*	*Incoherent*
1	0 - 11	1.28	0.70	1.07
2	12 - 23	1.24	0.45	1.15
3	24 - 35	1.10	0.33	1.06
4	36 - 47	1.48	0.72	1.29
5	48 - 59	1.18	0.43	1.10
6	60 - 71	1.20	0.47	1.11
7	74 - 83	1.19	0.59	1.04
8	84 - 95	1.44	0.95	1.07
9	96 - 107	1.59	1.04	1.20
10	108 - 119	1.34	0.61	1.19

Table 7.16: Averages across time samples for Run 1 - la0716.seq4.

Chip	*Channels*	*Total Noise*	*Coherent*	*Incoherent*
1	0 - 11	1.31	0.71	1.10
2	12 - 23	1.28	0.39	1.22
3	24 - 35	1.13	0.36	1.07
4	36 - 47	1.52	0.68	1.36
5	48 - 59	1.24	0.52	1.12
6	60 - 71	1.23	0.49	1.13
7	74 - 83	1.23	0.62	1.05
8	84 - 95	1.44	0.90	1.13
9	96 - 107	1.61	1.06	1.21
10	108 - 119	1.36	0.60	1.22

Table 7.17: Averages across time samples for Run 2 - la0719.seq7.

The total noise of each of the 10 chips during the pedestal tests ranged from 1.1 to 1.6 ADC counts. The coherent noise ranged from 0.33 to 1.06 ADC counts. The incoherent noise ranged from 1.0 to 1.4 ADC counts.

Chip 3 had the least coherent noise, averaged over time samples. In Run 1, Chip 3 had a coherent noise of 0.33 ADC counts, and in Run 2, Chip 3 had a coherent noise of 0.36 ADC counts. Chip 9 had the most coherent noise, averaged over time samples. In Run 1, Chip 9 had a coherent noise of 1.04 ADC counts, and in Run 2, Chip 9 had a coherent noise of 1.06 ADC counts.

The average total noise of each chip in Run 1 is 1.3 ADC counts. The average coherent and incoherent noise of each board in Run 1 is 0.63 ADC counts and 1.1 ADC counts respectively. For Run 2, the average total noise, coherent noise and incoherent noise values are 1.3 ADC counts, 0.63 ADC counts and 1.2 ADC counts respectively.

The total noise and incoherent noise in Run 2 was greater than Run 1 for all 10 chips, and the coherent noise was roughly the same in each run.

7.4.7 Conclusions

The incoherent noise of the pipeline system is estimated to be between 1.0 and 1.4 ADC counts. The coherent noise over channels for the whole system was estimated to be about 0.33 ADC counts.

The coherent noise over channels for each board is estimated to be 0.47 ADC counts.

The coherent noise over channels for each chip is estimated to be 0.63 ADC counts.

Thus, it appears that the largest coherent noise exists across channels of individual chips. This means that there is some electronic noise within SCA chips which causes all of the channels of a single chip to shift simultaneously.

CHAPTER 8

Exposure of SCA Chips to Radiation

Although the front-end boards will be located in relatively low radiation areas (approximately 2.5 krad/year) when used in the ATLAS detector, it is essential to know the effects of radiation on the board components. This chapter details two experiments which were performed to determine the response of SCA chips to radiation. The first experiment consisted of exposing SCA chips to electron and proton beams at CERN in 1994. The second experiment consisted of placing SCA chips near a gamma-ray source at the University of Alberta in 1995.

8.1 Electron and Proton Radiation Effects

In order to determine the sensitivity of switched capacitor array (SCA) chips to radiation, several chips were exposed to the proton beam of the PS (Proton Synchrotron) and the electron beam of the LIL (LEP Injector Linac) at CERN during June 11 - July 7, 1994. Also, in order to understand any dependence on temperature, and to check for annealing, some SCA chips were operated in an oven. The tests[1], and the conclusions drawn about the radiation and temperature sensitivity of the switched capacitor array chips, are described [31]. The energy of protons from the PS was 27 GeV, and the energy of electrons from the LIL was 600 MeV.

[1]The tests were performed by Bryan Caron, Robert Davis, Lars Holm and Shane Mullin.

8.1.1 Introduction

A simple readout PC board was assembled for the tests. Different SCA chips could be plugged into a single socket on the board. Four of the 16 SCA channels were multiplexed through two 12-bit ADCs. A separate controller provided a random read address allowing a single capacitor in each channel to be read out at a rate of approximately 200 Hz. The full scale of the SCA chips in this test was 4096 ADC counts.

A proton beam from the PS or electron beam from LIL could be directed onto the SCA chip during operation and the beam flux measured. Tests were performed by running the SCA with or without a DC voltage applied to the inputs. The readout board could also be operated in an oven with an accuracy of $\pm 3°C$ to study the temperature sensitivity and possible annealing of the chip.

8.1.2 Observations

It was observed that when a SCA chip has voltage applied, about 0.2% of the ADC counts are approximately 100 counts above pedestal. These counts are significantly different from the others and are thought to be due to an error in the SCA chip.

8.1.3 Effects of Proton Irradiation and Annealing

Baseline (no radiation) runs, using SCA chips both with and without voltage applied, were performed. It was determined that the rms noise is lower when a voltage is applied. Also, about half of the pedestal noise is due to tails in the ADC distributions.

A chip under voltage was irradiated with the proton beam from the PS. The

number of ADC counts dropped to zero in all channels. Then, under continued irradiation, the number of ADC counts in all channels rose above the baseline voltage; two of the channels even saturated. When the beam was turned off, the number of ADC counts in all channels slowly returned towards the applied voltage. It was determined that irradiation removed the tails in the ADC distributions when voltage was applied to the chip.

The same procedure was repeated for a chip with no voltage applied. Irradiation caused the number of ADC counts in all channels to rise above the baseline voltage. Again, two of the channels saturated. When the beam was turned off, the number of ADC counts in all channels again slowly returned towards their initial values.

The number of ADC counts versus event number (time) for these proton irradiation runs, with and without voltage applied, are shown in Figures 8.1 and 8.2 respectively. The chip was irradiated for a total of 0.8 hours and received 1.5×10^{13} protons/cm^2. The total absorbed dose is estimated to be 0.5 Mrad.

A series of heating runs were performed on a SCA chip after it had been irradiated by protons. The noise increased while the chip was being heated. After heating and cool-down, the pedestal counts were close to the baseline counts, but still significantly different. The noise was the same as before heating.

About 89 hours after this chip had been irradiated and an attempt at annealing had been made, the pedestal ADC counts had recovered to within about 30 counts of the baseline pedestal counts, and the voltage ADC counts to within 120 counts of the baseline voltage counts. The pedestal noise decreased by about 24% from the baseline pedestal noise, but the voltage noise increased by a factor of six from the baseline voltage noise. About half of the noise when voltage is applied is due to tails

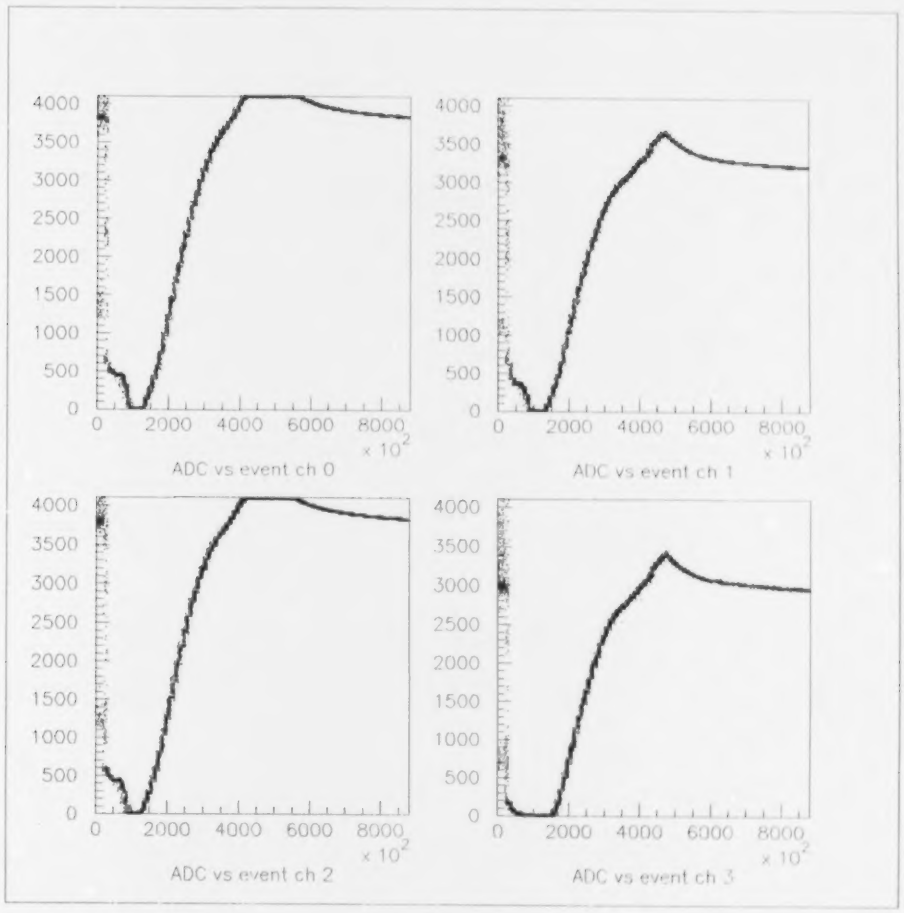

Figure 8.1: Number of ADC counts versus event number (time) for the proton irradiation run, with voltage applied.

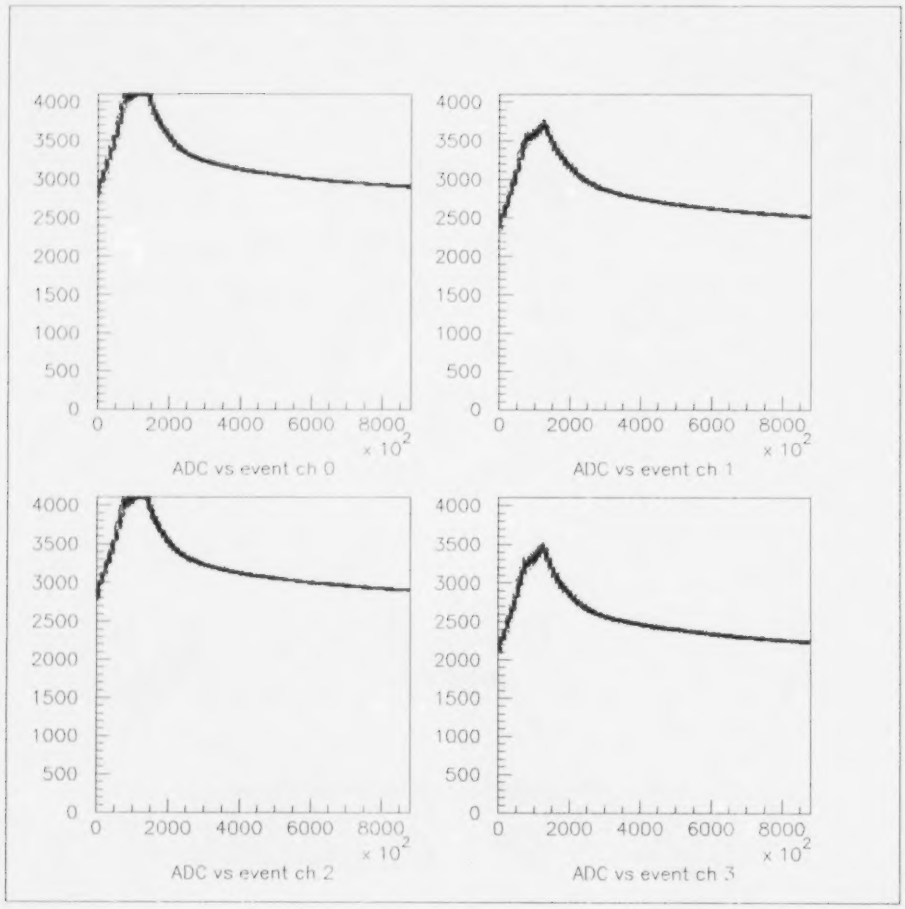

Figure 8.2: Number of ADC counts versus event number (time) for the proton irradiation run, without voltage applied.

in the ADC distributions.

8.1.4 Effects of Electron Irradiation

Baseline (no radiation) runs, both with and without voltage applied to a SCA chip, were performed. Again, the noise was higher when voltage was applied, and about half of the pedestal noise was due to tails in the ADC distributions.

The SCA chip was irradiated with the electron beam from LIL, and received a flux of 5.285×10^{12} electrons/cm^2 over about 1.8 hours.. With voltage applied to the chip, the ADC counts in all channels dropped quickly to about 100 counts after irradiation. The noise increased significantly just before the number of ADC counts began to drop. The tails in the ADC distributions merged with the mean ADC counts while and after the chip began to fail. Figure 8.3 shows the number of ADC counts versus event number (time) for the electron irradiation run.

After electron irradiation was ceased, the chip was observed with voltage applied to see if it would recover. The number of ADC counts in each channel began to rise about 28 hours after irradiation. However, after two days, the number of ADC counts in each channel was still far below the baseline counts, and the noise was about an order of magnitude larger than the baseline noise. When voltage was applied to the chip, irradiation with electrons did not remove the tails in the ADC distributions. The chip was essentially damaged.

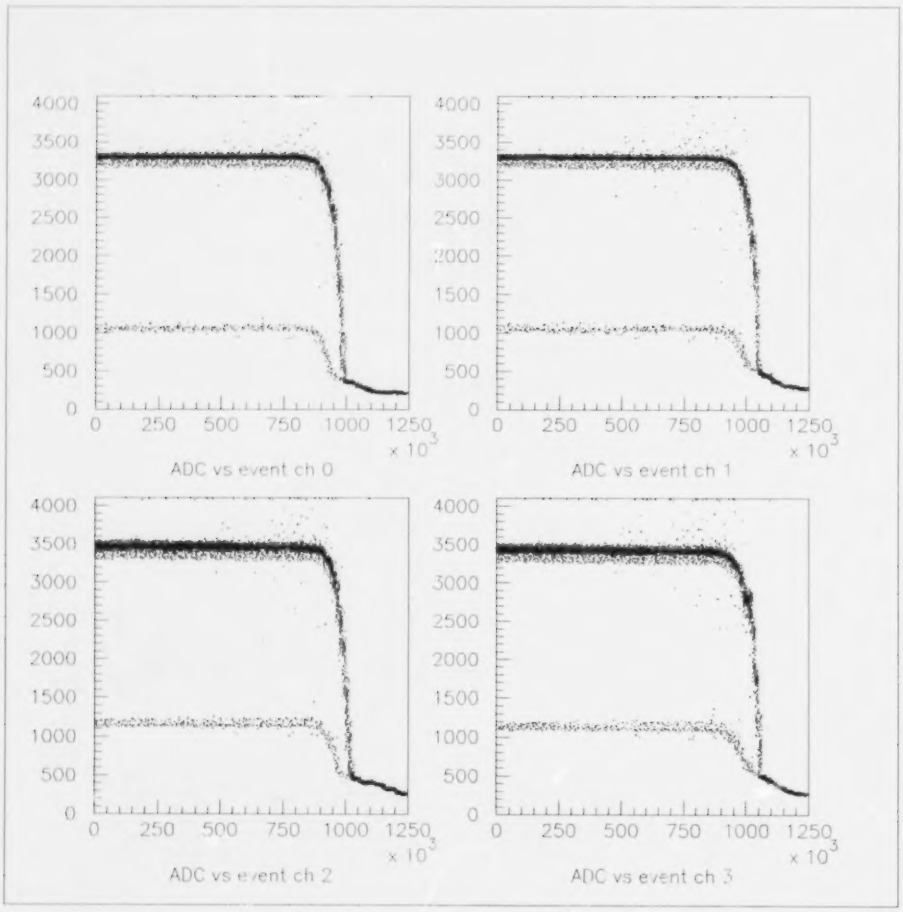

Figure 8.3: Number of ADC counts versus event number (time) for the electron irradiation run, with voltage applied.

8.1.5 Temperature Effects

Two baseline runs, both with and without voltage applied to a SCA chip, were performed. Again, about half of the pedestal noise was due to tails in the ADC distributions.

The SCA chip was placed into an oven with the voltage removed, and a series of pedestal tests were performed at different temperatures. In two of the four channels, the number of ADC counts jumped when the temperature rose to 50°C, and also when the temperature dropped to 35°C. Also, in these two channels, the pedestal counts increased and the noise roughly doubled after heating and cooling. However, in the other two channels, the pedestal and noise counts did not change after heating and cooling.

An additional pedestal run was performed at room temperature approximately 33 hours after heating. With voltage applied to the chip, the mean ADC counts decreased slightly after heating, while the noise did not change significantly. Heating the chip did not remove the tails in the ADC distributions.

8.1.6 Death of a SCA Chip

A SCA chip at pedestal voltage was irradiated by protons. After about 30 minutes, the chip died. During irradiation, the chip received a beam flux of 3.79×10^{12} protons/cm^2, which corresponds to an absorbed dose of about 0.3 Mrad. As before, the pedestal increased with irradiation. The number of ADC counts versus event number (time) for the severe proton irradiation run is shown in Figure 8.4.

An attempt was made to recover the dead SCA chip through annealing. It was placed, under voltage, into an oven, and the temperature was increased from

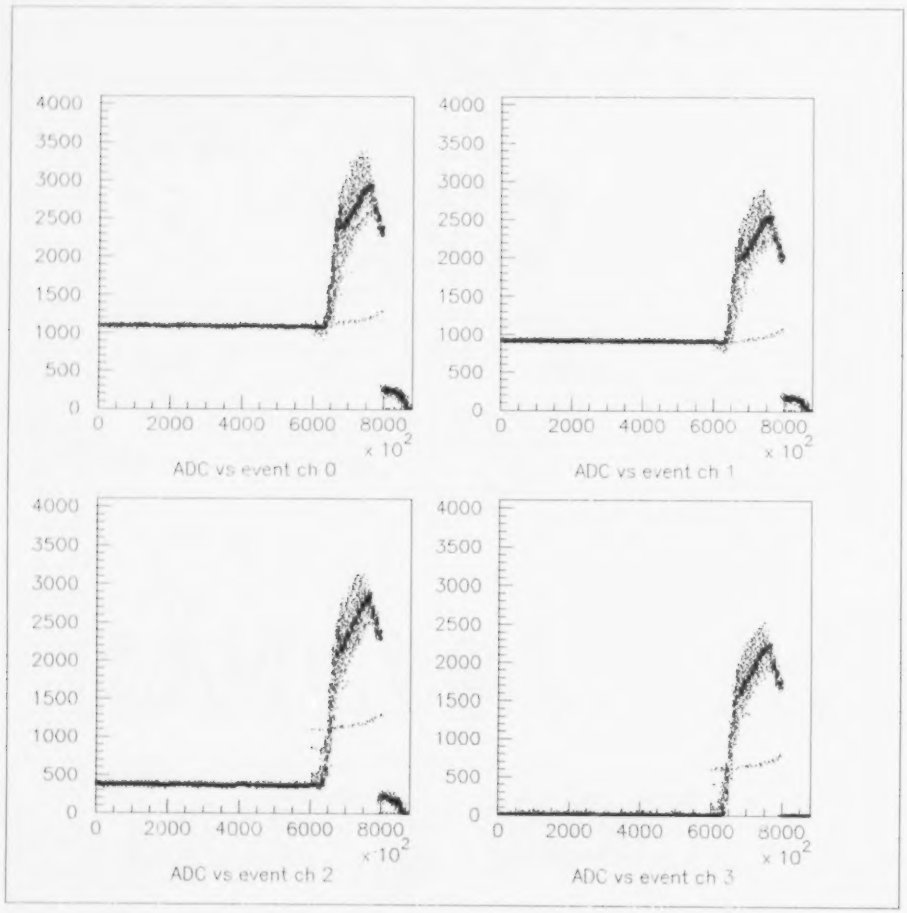

Figure 8.4: Number of ADC counts versus event number (time) for a proton irradiation run in which the SCA chip, operated at pedestal voltage, died.

30°C to 60°C, and then decreased to less than 38°C. The annealing process increased the number of ADC counts and decreased the noise, but the chip did not completely recover.

A different SCA chip, also at pedestal voltage, was irradiated by electrons. The chip received a beam flux of 5.285×10^{12} electrons/cm^2. After electron irradiation, the chip was observed both without and with voltage applied. In both cases, almost all of the capacitors in all the channels had saturated ADC counts. Also, it appeared that the addressing had failed for six capacitors in each channel. This SCA chip, with no bias voltage applied during electron irradiation, was badly damaged.

8.1.7 Conclusions

The SCA chips were clearly affected by radiation and temperature. If a chip was still functioning after irradiation, the pedestals and gains had changed. Chips did not completely recover from irradiation after long periods of time. Attempts to recover dead or almost dead chips (after irradiation) by annealing failed. Heating a chip that had not been irradiated changed the pedestals and gains by a small amount. While the noise in some channels was not affected by heating, other channels showed significant noise increases.

8.2 Exposure to Gamma Radiation

Switched capacitor array chips were exposed to a Cobalt-60 source at the University of Alberta during July-December, 1995. Results which demonstrate the sensitivity of the switched capacitor array to gamma radiation are presented.

8.2.1 Introduction

The readout system used for these tests was the same as for the electron and proton radiation experiment at CERN, involving a simple PC readout board. Different switched capacitor array chips could be plugged into a single socket on the board. Four of the 16 SCA channels were multiplexed through two 12-bit ADCs. A separate controller provided a random read address allowing a single capacitor in each channel to be read out at a rate of approximately 500 Hz. The full scale of the SCA chips in this test was 4096 ADC counts.

In total, 525 data files, each consisting of 500,000 events, were recorded for four different SCA chips, called Chip A, Chip B, Chip C and Chip D. Data files were recorded every several hours. For each chip, baseline data were recorded prior to irradiation, then data were recorded during irradiation, and finally data were recorded once irradiation had ceased.

The entire readout board was enclosed in lead, in order to shield it from the radiation. The front wall of lead was 15 centimeters thick, and this thickness of lead would reduce the dose rate by a factor of 2×10^4. Gamma rays from the Cobalt-60 source were directed onto the SCA chip during operation by means of a hole ($\frac{1}{2}$ inch diameter) drilled through the lead. Photons are emitted from the source with an energy of either 1.173 MeV or 1.333 MeV. For Chips A and B, the distance from the

Cobalt-60 source to the SCA chip was measured to be 109 cm. Fricke dosimetry[2] was performed to determine the amount of radiation passing through the SCA chip at this distance. The dose rate was measured to be 81 rad/hour. Chip C was placed at a distance of 57 cm from the source. The dose rate at this distance was measured to be 113 rad/hour. Chip D was placed at a distance of 73 cm from the source. The dose rate at this distance was measured to be 86 rad/hour. Two of the SCA channels were operated with a DC voltage applied to the inputs, and two of the SCA channels were operated without a DC voltage. The air temperature around the readout board was recorded periodically, and any changes were noted.

For each of the 256 capacitors in each channel, a distribution of the number of ADC counts was accumulated, and the mean and rms deviation calculated. The tails of the ADC distribution were truncated $\pm$ 10 ADC counts around the mean values for each capacitor to exclude outliers, and the mean and rms deviation were recalculated. In the case of Chip A, this resulted in about 1% of the data being cut. For Chips B, C and D, approximately 0.5% of the data were cut. Throughout this chapter, the mean ADC counts for each channel is the mean ADC counts over all capacitors in the channel. The noise for each channel is an average of the rms deviations of all of the capacitors in the channel.

The following sections present the empirical results of the tests for each of the

[2]Dosimetry was performed by Dr. Yixing Zhao of the Department of Chemistry, University of Alberta. Fricke solution (0.0975 g of $Fe(NH_3)_2(SO_4)_2 \cdot 6H_2O$ dissolved in Nanopure water + 11 ml of concentrated H_2SO_4 + Nanopure water to make a total volume of 250 ml) was poured into three quartz cells, each with a volume of 3 ml. The absorbence of each of the three solutions was measured, using a UV-Spectrophotometer at 304 nm. Two of the cells were placed at the front and back of the SCA chip prior to irradiation, and the third cell was kept as a reference. After radiation was ceased, the absorbences of the irradiated solutions and the reference solution were again measured. The irradiation dose (D) absorbed in the solutions was calculated using the equation: $D = 2.76 \times 10^4 \times \Delta A$, where ΔA is the absorbence difference between the reference and irradiated solutions at room temperature. The dose rate at the SCA chip was taken to be the average of the dose rates of the two irradiated solutions [32].

four chips.

8.2.2 Chip A

In total, 162 data files were recorded for Chip A, over a four week period. Eighteen files were recorded before irradiation, 113 during irradiation, and 31 after irradiation. In terms of time, Chip A was analyzed for three days prior to irradiation, 14 days during irradiation, and eight days after irradiation. Chip A was irradiated for a total of 321 hours, and the total absorbed dose was determined to be 27 krad. Data files were recorded every 2 - 6 hours. Four channels of the SCA chip were used. Channels 0 and 2 had no voltage applied (pedestal), and Channels 1 and 3 had a DC voltage applied. The data acquisition rate was 3 kHz initially, but was changed to 0.5 kHz after seven days of irradiation, for reasons discussed later.

The number of ADC counts versus time (minutes) for the entire run with Chip A is shown in Figure 8.5 for all four channels. Each point represents the average number of ADC counts for a 500,000 event file recorded at the corresponding time. "On" and "off" denote the points at which irradiation was started and ceased, respectively.

The number of ADC counts in all four channels decreased slightly during the first days of irradiation. Then, after 8 days of irradiation, the number of ADC counts behaved erratically in all four channels for two days. At the time that this erratic behavior began, the chip had received a total of about 15 krad.

In each of the pedestal channels (0 & 2), the number of ADC counts seemed to fluctuate in a periodic manner, changing by as much as 20%, over the next two days. Then, the number of ADC counts was fairly constant for about three days, at which point it started to decrease steadily. The irradiation was ceased shortly thereafter.

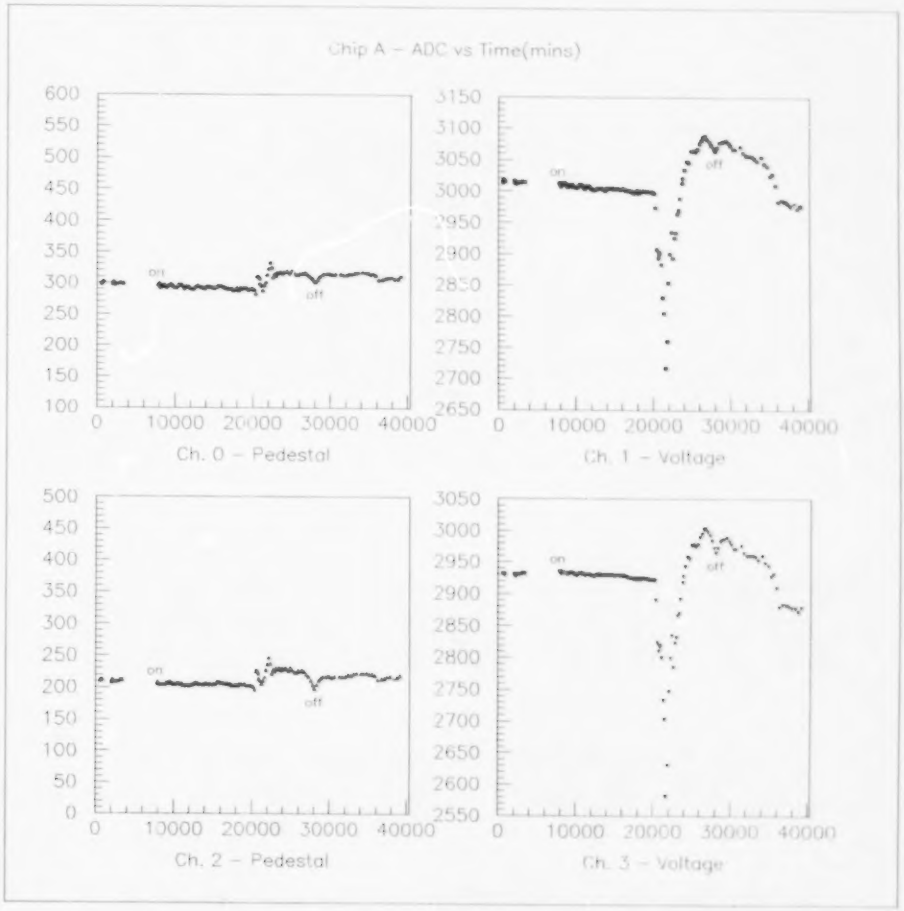

Figure 8.5: Mean number of ADC counts versus time (minutes) for Chip A.

In each of the voltage channels, (1 & 3), the number of ADC counts decreased very rapidly for one day to about 85% of the original value, and then immediately increased rapidly for two days to a value which is about 3% greater than the original value. Then, the number of ADC counts increased less rapidly for one day, before beginning a steady decrease. At this point, irradiation was ceased.

After irradiation, the number of ADC counts increased in all four channels for about one day. Then, in each of the pedestal channels, the number of ADC counts seemed to remain fairly constant for five days, before assuming a slightly lower value for the final two days of the run. However, in each of the voltage channels, the number of ADC counts decreased by about 3% over a five day period, before leveling out for the last two days of the run.

Table 8.1 shows the number of ADC counts in each channel before irradiation, before the erratic period, after irradiation, and at the end of the run, for Chip A.

Channel	*Before Irradiation*	*Before Erratic Period*	*After Irradiation*	*At End of Run*
Ch. 0 - Pedestal	298.3	287.7	300.3	310.1
Ch. 1 - Voltage	3013.6	2996.1	3063.5	2976.9
Ch. 2 - Pedestal	211.1	200.2	198.1	218.8
Ch. 3 - Voltage	2931.4	2921.4	2964.3	2878.7

Table 8.1: Number of ADC counts for all four channels at various points in the run, for Chip A.

Table 8.2 shows the minimum and maximum number of ADC counts achieved during the erratic period for all four channels.

A plot of the noise versus time (minutes) for the entire run with Chip A is shown in Figure 8.6 for all four channels. Each point represents the rms noise of a 500,000 event file recorded at the corresponding time.

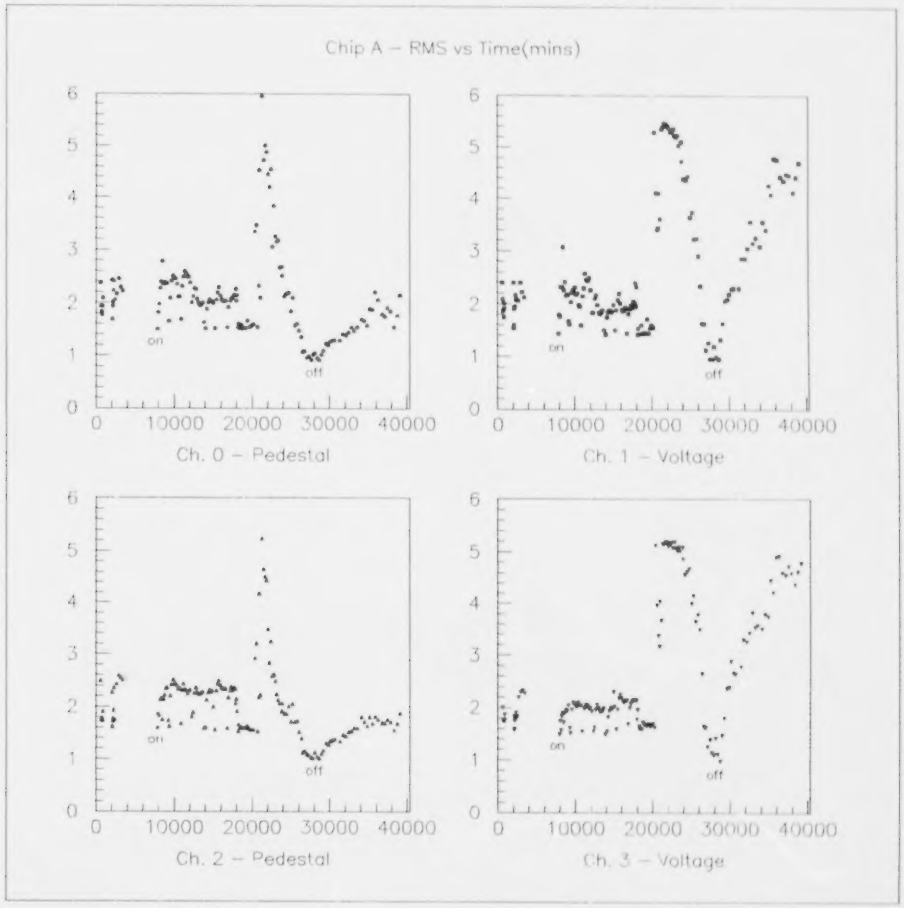

Figure 8.6: RMS noise (ADC counts) versus time (minutes) for Chip A.

The rms noise in all four channels is somewhat inconsistent before irradiation and during the first seven days of irradiation. Some of the files were less noisy then the rest, by about 1 ADC count. However, most of the files exhibited the higher noise

value. This inconsistency may be due to the program which was used to record the data. It is thought that the rate was greater than the program could accept. Initially, the noise pulser rate was 3 kHz. This was changed to about 0.5 kHz after seven days of irradiation. It can be seen in the plots that the lower data acquisition rate caused the rms values in all four channels to drop.

After eight days of irradiation, the noise values behaved quite erratically. In all four channels, the rms noise increased very quickly from about 1.5 ADC counts to over five ADC counts. Over the next two days, the rms noise in each of the pedestal channels dropped steadily to a low of about 1 ADC count. Meanwhile, the noise in each of the voltage channels remained above 5 ADC counts for one day before decreasing rapidly to around 1 ADC count. Irradiation was ceased at this point.

The rms noise in all four channels remained at around 1 ADC count for about a day before it started to increase in all four channels. In each of the two pedestal channels, the noise increased over the next five days, to a value of about 1.7 ADC counts. In each of the voltage channels, however, the noise increased during this time to about 4.5 ADC counts. During the final two days of the run, the rms noise in each of the four channels remained close to these values.

Table 8.3 shows the rms noise in ADC counts in each channel before irradiation, before the erratic period, after irradiation, and at the end of the run, for Chip A. Because it is suspected that many of the noise values before irradiation were inflated by a problem with the data acquisition program, both a high value and a low value are shown in this column in Table 8.3.

Table 8.4 shows the minimum and maximum rms noise achieved during the erratic period for all four channels.

Throughout the entire run with Chip A, the air temperature within the lead

Channel	*Minimum*	*Maximum*
Ch. 0 - Pedestal	281.7	331.6
Ch. 1 - Voltage	2716.6	3087.3
Ch. 2 - Pedestal	196.1	246.4
Ch. 3 - Voltage	2580.7	3003.2

Table 8.2: Minimum and maximum number of ADC counts achieved during the erratic period, for Chip A.

Channel	*Before Irradiation*	*Before Erratic Period*	*After Irradiation*	*At End of Run*
Ch. 0 - Pedestal	2.22/1.69	1.59	0.95	1.76
Ch. 1 - Voltage	2.12/1.60	1.55	0.99	4.41
Ch. 2 - Pedestal	2.50/1.61	1.55	1.04	1.67
Ch. 3 - Voltage	2.27/1.60	1.63	1.11	4.61

Table 8.3: RMS noise in ADC counts for all four channels at various points in the run, for Chip A.

shielding (*ie.* the location of the readout board) was 26 $\pm$ 1 degrees Celsius. It appears that the lead enclosure not only protected the board components, but also helped to maintain a constant temperature.

8.2.3 Chip B

In total, 186 data files were recorded for Chip B; 40 before irradiation, 97 during irradiation, and 49 after irradiation. In terms of time, Chip B was analyzed for four days prior to irradiation, 19 days during irradiation, and 13 days after irradiation. Chip B was irradiated for a total of 450 hours, and the total absorbed dose was determined to be 38 krad. Data files were recorded every 2 - 6 hours, in general. Four channels of the SCA Chip were used. Channels 0 and 2 had no voltage applied (pedestal), and Channels 1 and 3 had a DC voltage applied. The data acquisition rate was maintained at 500 Hz.

The number of ADC counts versus time (minutes) for the entire run with Chip B is shown in Figure 8.7 for all four channels. Each point represents the average number of ADC counts for a 500,000 event file recorded at the corresponding time.

The number of ADC counts in each of the four channels decreased very slightly or remained constant during the first days of irradiation. Then, after 7 days of irradiation, the number of ADC counts behaved erratically in all four channels for two to four days. At the time that this erratic behavior began, the chip had received a total of about 15 krad.

In each of the pedestal channels (0 & 2), the number of ADC counts seemed to fluctuate in a periodic manner, changing by as much as 10%, over the next two days. Then, the number of ADC counts returned to its original value, and then continued

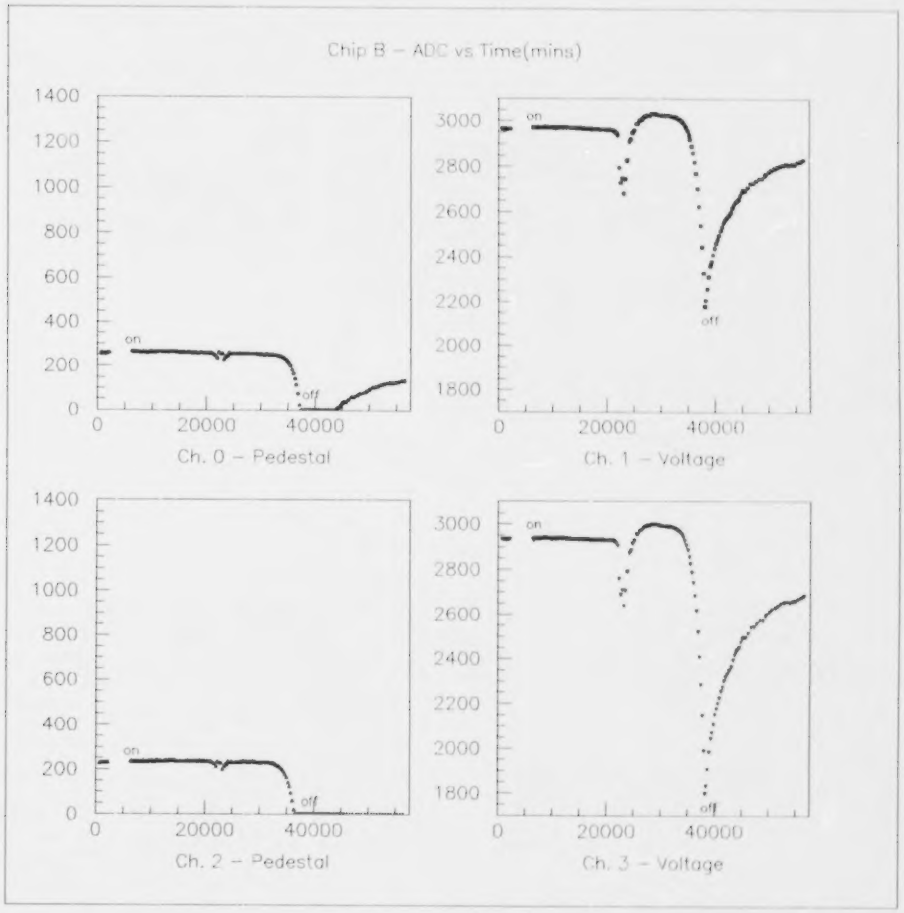

Figure 8.7: Mean number of ADC counts versus time (minutes) for Chip B.

to decrease slightly over the next 6 days.

In each of the voltage channels, (1 & 3), the number of ADC counts decreased very rapidly for one day to about 90% of the original value, and then immediately increased rapidly for three days to a value which is about 3% greater than the original value. Then, the number of ADC counts decreased slightly over the next four days.

After 15 days of irradiation, the number of ADC counts in all four channels dropped rapidly. The drop continued in all four channels for three days, at which point irradiation was ceased. The pedestal channels (0 & 2) reached zero after two days, and the voltage channels (1 & 3) dropped to 73% and 60% of their original value, respectively. This rapid drop began when Chip B had received a total of 29 krad.

Immediately after irradiation was ceased, the number of ADC counts in each of the voltage channels (1 & 3) increased rapidly. This increase continued until the end of the run, although it seemed to be leveling off.

Pedestal channel 0 remained at zero for three days after irradiation was ceased. Then, the number of ADC counts steadily increased for the remainder of the run, however it appeared to be leveling off near the end.

After irradiation was ceased, the number of ADC counts in pedestal channel 2 remained at zero until the end of the run.

Table 8.5 shows the number of ADC counts in each channel before irradiation, before the erratic period, after the erratic period, and before the large drop, for Chip B.

Table 8.6 shows the minimum and maximum number of ADC counts achieved during the entire run for all four channels.

Channel	*Minimum*	*Maximum*
Ch. 0 - Pedestal	0.91	5.95
Ch. 1 - Voltage	0.95	5.46
Ch. 2 - Pedestal	1.01	5.23
Ch. 3 - Voltage	0.98	5.19

Table 8.4: Minimum and maximum rms noise achieved during the erratic period, for Chip A.

Channel	*Before Irradiation*	*Before Erratic Period*	*After Erratic Period*	*Before Drop*
Ch. 0 - Pedestal	261.4	256.1	254.7	250.1
Ch. 1 - Voltage	2969.1	2959.1	3030.4	3021.8
Ch. 2 - Pedestal	233.5	235.4	232.8	228.8
Ch. 3 - Voltage	2934.8	2927.2	2998.0	2987.4

Table 8.5: Number of ADC counts for all four channels at various points in the run, for Chip B.

A plot of the noise versus time (minutes) for the entire run with Chip B is shown in Figure 8.8 for all four channels. Each point represents the rms noise of a 500,000 event file recorded at the corresponding time.

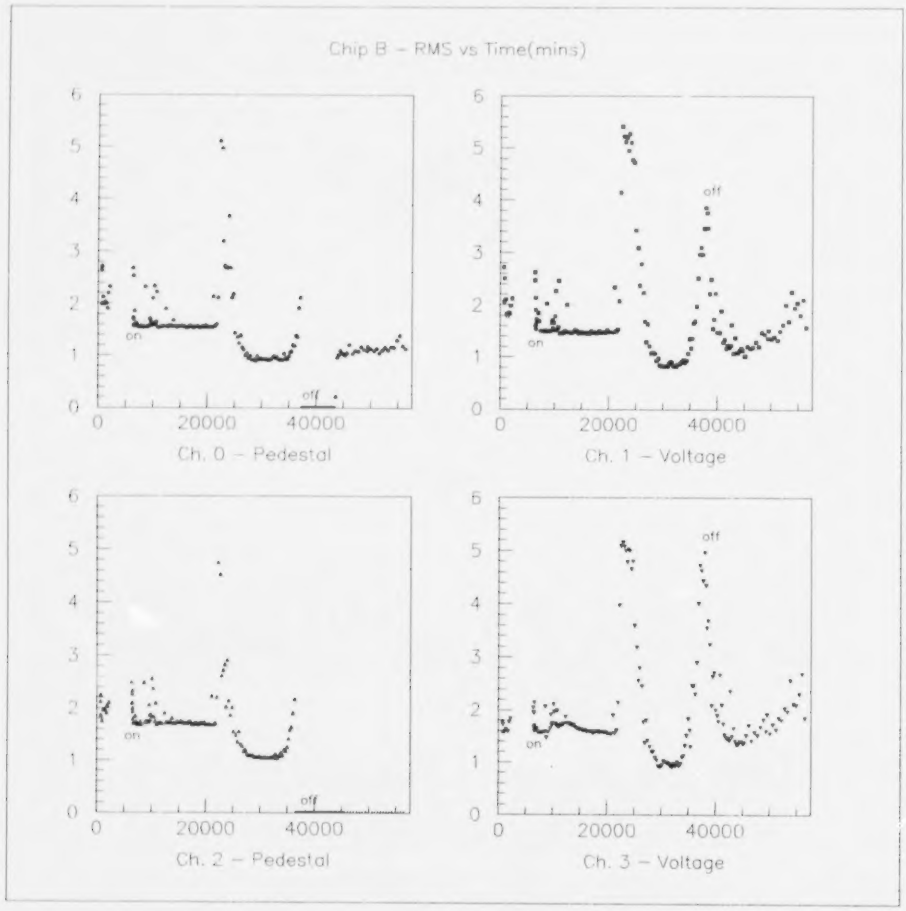

Figure 8.8: RMS noise (ADC counts) versus time (minutes) for Chip B.

The rms noise in all four channels was slightly inconsistent prior to irradiation. Some of the data files are noisier than the rest. However, most of the data files have similar values for rms noise (1.5 - 1.7 ADC counts), in each of the four channels.

After about 7 days of irradiation, the noise in each of the four channels increased rapidly for one day, to a high of about five ADC counts. Then, the rms noise decreased for two days, before leveling off at about 1 ADC count.

In each of the pedestal channels (0 & 2), the rms noise remained at around 1 ADC count for about four days, and then increased rapidly for one day. Then, the rms noise values were all zero, because the two pedestal channels were both reading zero at this point.

In the two voltage channels (1 & 3), the rms noise remained at around 1 ADC count for about three days, and then increased rapidly for two days to highs of 4 and 5 ADC counts respectively, at which point irradiation was ceased.

Immediately after irradiation was ceased, the rms noise in each of the voltage channels (1 & 3) decreased rapidly for two days to about 1.2 and 1.5 ADC counts respectively. Then, the rms noise in both channels increased steadily for the remainder of the run.

The rms noise of pedestal channel 0 remained at zero for about three days after irradiation, at which point Channel 0 began to read non-zero ADC values. The rms noise was then about 1.0 ADC counts, and increased slightly for the remainder of the run.

Pedestal Channel 2 never recovered after irradiation, and so has a noise of 0.0 ADC counts for the remainder of the run.

Table 8.7 shows the rms noise in ADC counts in each channel before irradiation, before the erratic period, after the erratic period, and at the end of the run, for Chip B.

Table 8.8 shows the minimum and maximum rms noise achieved during the

Channel	*Minimum*	*Maximum*
Ch. 0 - Pedestal	0.0	264.5
Ch. 1 - Voltage	2181.0	3030.5
Ch. 2 - Pedestal	0.0	239.2
Ch. 3 - Voltage	1799.5	2998.7

Table 8.6: Minimum and maximum number of ADC counts achieved during the entire run, for Chip B.

Channel	*Before Irradiation*	*Before Erratic Period*	*After Erratic Period*	*At End of Run*
Ch. 0 - Pedestal	1.65	1.57	0.99	1.30
Ch. 1 - Voltage	1.57	1.49	0.97	2.04
Ch. 2 - Pedestal	1.74	1.69	1.06	0.00
Ch. 3 - Voltage	1.70	1.56	1.04	2.09

Table 8.7: RMS noise in ADC counts for all four channels at various points in the run, for Chip B.

entire run for all four channels, excluding files in which the number of ADC counts was 0.

Channel	*Minimum*	*Maximum*
Ch. 0 - Pedestal	0.89	5.11
Ch. 1 - Voltage	0.82	5.40
Ch. 2 - Pedestal	1.04	4.74
Ch. 3 - Voltage	0.90	5.15

Table 8.8: Minimum and maximum rms noise achieved during the entire run, for Chip B.

Throughout the entire run with Chip B, the air temperature within the lead shielding was 27 $\pm$ 1 degrees Celsius.

8.2.4 Chip C

In total, 89 data files were recorded for Chip C, over a one month period. 31 files were recorded before irradiation, 35 during irradiation, and 23 after irradiation. In terms of time, Chip C was analyzed for 15 days prior to irradiation, nine days during irradiation, and seven days after irradiation. Chip C was irradiated for a total of 211 hours, and the total absorbed dose was determined to be 24 krad. Data files were recorded every 6 or 12 hours. Four channels of the SCA chip were used. Channels 0 and 2 had no voltage applied (pedestal), and Channels 1 and 3 had a DC voltage applied. The data acquisition rate was maintained at around 350 Hz throughout the run.

The number of ADC counts versus time (minutes) for the entire run with Chip

C is shown in Figure 8.9 for all four channels. Each point represents the average number of ADC counts for a 500,000 event file recorded at the corresponding time. "On" and "off" denote the points at which irradiation was started and ceased, respectively.

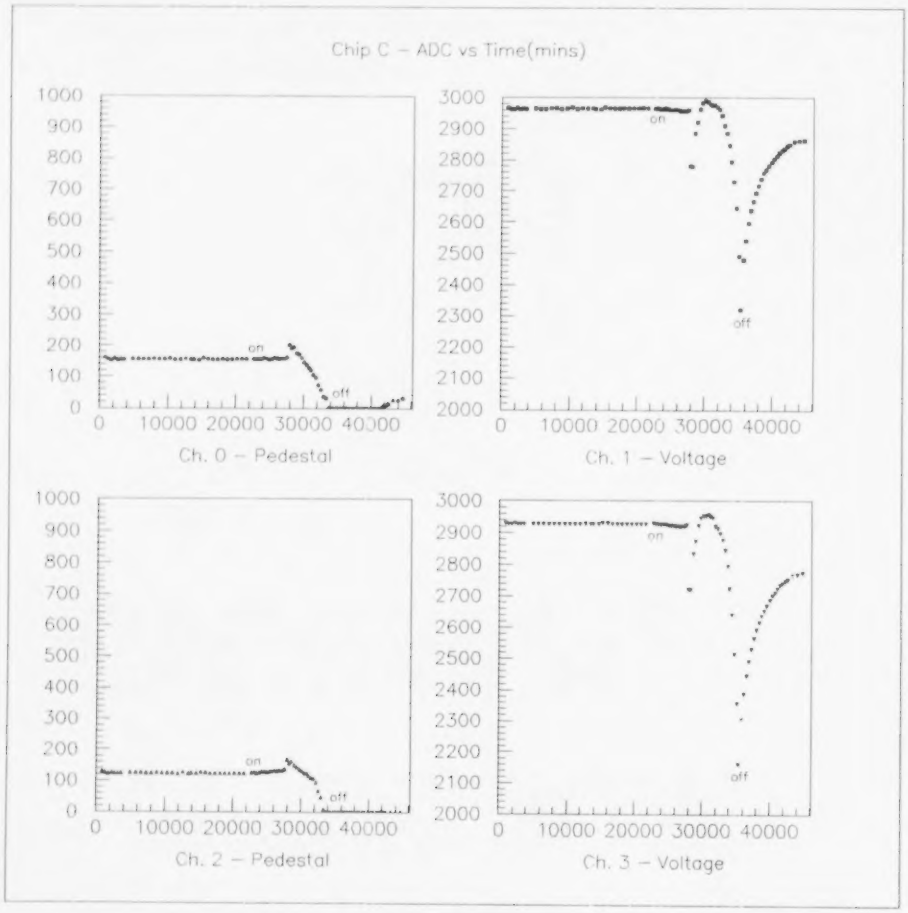

Figure 8.9: Mean number of ADC counts versus time (minutes) for Chip C.

The number of ADC counts in all four channels remained fairly constant during the 15 days prior to irradiation. During the first four days of irradiation, the number of ADC counts increased slightly in the pedestal channels, and decreased slightly in

the voltage channels. Then, after four days of irradiation, the number of ADC counts in all four channels behaved erratically. At the time that this erratic behavior began, the chip had received a total of about 9 krad.

In each of the pedestal channels, (0 & 2), the number of ADC counts increased abruptly by about 20%, and then steadily decreased over the next four days, until all capacitors in the pedestal channels read zero. The pedestal channels remained at zero for one day, at which point irradiation was ceased. Four days later, Channel 0 started to increase, and two days after that, Channel 2 started to increase.

In each of the voltage channels, (1 & 3), the number of ADC counts dropped abruptly to about 93% of the original value, and then increased rapidly for about two days to a value which is about 1.5% greater than the original value. Then, the number of ADC counts decreased very rapidly for about three days, at which point irradiation was ceased. Once irradiation was ended, the number of ADC counts in each of the voltage channels increased rapidly, but began to level off at a value which was about 5% less than the original value.

Table 8.9 shows the number of ADC counts in each channel before irradiation, before the erratic period, after irradiation, and at the end of the run, for Chip C.

Table 8.10 shows the minimum and maximum number of ADC counts achieved during the entire run, for all four channels.

A plot of the rms noise versus time (minutes) for the entire run with Chip C is shown in Figure 8.10 for all four channels. Each point represents the rms noise of a 500,000 event file recorded at the corresponding time.

The rms noise in all four channels fluctuates somewhat during the first ten

Channel	*Before Irradiation*	*Before Erratic Period*	*After Irradiation*	*At End of Run*
Ch. 0 - Pedestal	155.4	157.0	0.0	30.5
Ch. 1 - Voltage	2964.3	2956.1	2321.1	2862.4
Ch. 2 - Pedestal	122.1	131.7	0.0	0.8
Ch. 3 - Voltage	2926.5	2919.5	2160.4	2775.3

Table 8.9: Number of ADC counts for all four channels at various points in the run, for Chip C.

Channel	*Minimum*	*Maximum*
Ch. 0 - Pedestal	0.0	201.6
Ch. 1 - Voltage	2321.1	2989.3
Ch. 2 - Pedestal	0.0	166.5
Ch. 3 - Voltage	2160.4	2955.8

Table 8.10: Minimum and maximum number of ADC counts achieved during the entire run, for Chip C.

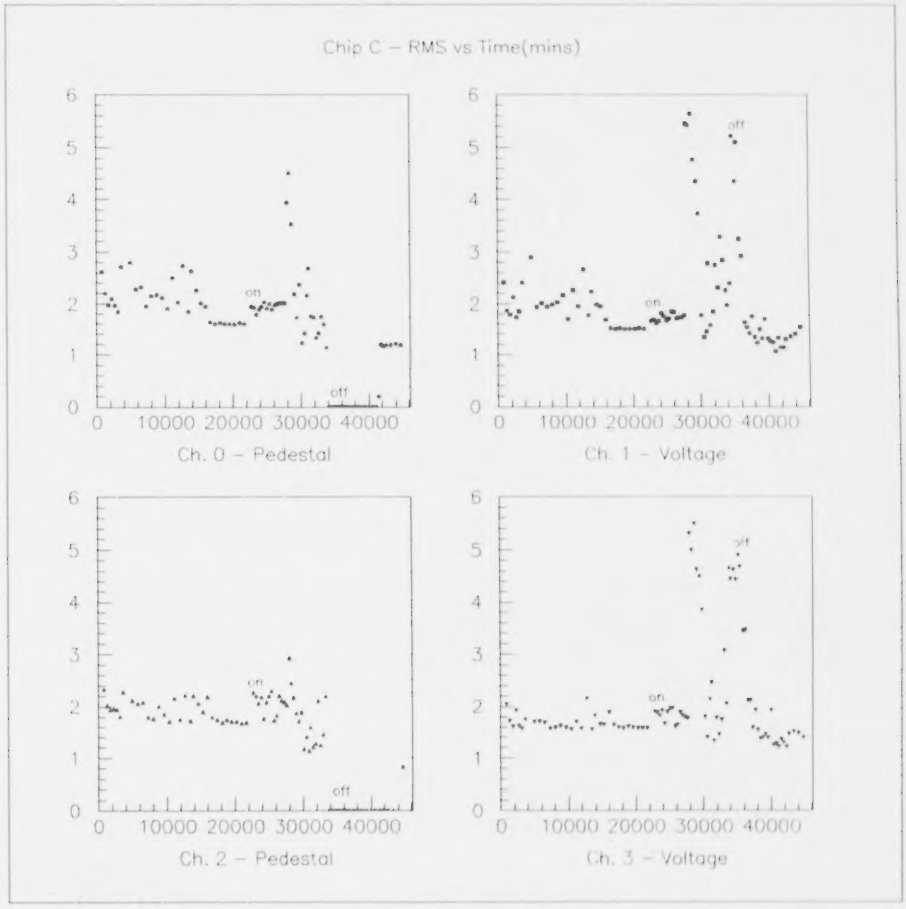

Figure 8.10: RMS noise (ADC counts) versus time (minutes) for Chip C.

days of the run. At this point, the data acquisition rate was turned down to about 350 Hz, and this stabilized the rms noise at 1.6 or 1.7 ADC counts in all four channels.

Once irradiation commenced, the rms noise increased abruptly in all four channels by 0.3 or 0.4 ADC counts. The rms noise remained at this level for about three and a half days, until the erratic period began.

In the pedestal channels (0 & 2), the rms noise increased abruptly to 4.5 and 2.9 ADC counts respectively. The rms noise fluctuated considerably but overall decreased during the next four days in both pedestal channels. Then, the rms noise values were zero, because the two pedestal channels were both reading zero at this point. After one day of zero readings, irradiation was ceased.

In the two voltage channels (1 & 3), the rms noise increased abruptly to 5.6 and 5.5 ADC counts respectively. Over the next two days, the rms noise of each of the voltage channels decreased rapidly to values that were slightly less than those prior to irradiation. Then, the rms noise increased rapidly for three days, at which point irradiation was ceased.

Four days after irradiation was ceased, pedestal channel 0 recovered, and the rms noise was fairly constant at 1.2 ADC counts. Pedestal channel 0 did not recover in time to allow for the determination of a value for the rms noise.

Immediately after irradiation was ceased, the rms noise in each of the voltage channels (1 & 3) decreased rapidly for two days to about 1.3 and 1.4 ADC counts respectively. The rms noise in both channels fluctuated somewhat but remained near these values for the remainder of the run.

Table 8.11 shows the rms noise in ADC counts in each channel before irradiation, before the erratic period, after the erratic period, and at the end of the run, for

Chip C.

Channel	*Before Irradiation*	*Before Erratic Period*	*After Erratic Period*	*At End of Run*
Ch. 0 - Pedestal	1.60	2.01	1.73	1.19
Ch. 1 - Voltage	1.50	1.73	1.84	1.54
Ch. 2 - Pedestal	1.69	2.08	1.28	N/A
Ch. 3 - Voltage	1.58	1.79	1.78	1.40

Table 8.11: RMS noise in ADC counts for all four channels at various points in the run, for Chip C.

Table 8.12 shows the minimum and maximum rms noise achieved during the entire run for all four channels, excluding files in which the number of ADC counts was zero.

Channel	*Minimum*	*Maximum*
Ch. 0 - Pedestal	1.16	4.50
Ch. 1 - Voltage	1.06	5.63
Ch. 2 - Pedestal	1.14	2.93
Ch. 3 - Voltage	1.22	5.49

Table 8.12: Minimum and maximum rms noise achieved during the entire run, for Chip C.

Throughout the entire run with Chip C, the air temperature within the lead shielding was 24 $\pm$ 1 degrees Celsius.

8.2.5 Chip D

In total, 88 data files were recorded for Chip D, over a three week period. 23 files were recorded before irradiation, 40 during irradiation, and 25 after irradiation. Chip D was analyzed for six days prior to irradiation, 10 days during irradiation, and six days after irradiation. Chip D was irradiated for a total of 244 hours, and the total absorbed dose was determined to be 21 krad. Data files were recorded every six hours. Four channels of the SCA chip were used. Channels 0 and 2 had no voltage applied (pedestal), and Channels 1 and 3 had a DC voltage applied. The data acquisition rate was about 900 Hz.

The number of ADC counts versus time (minutes) for the entire run with Chip D is shown in Figure 8.11 for all four channels. Each point represents the average number of ADC counts for a 500,000 event file recorded at the corresponding time. "On" and "off" denote the points at which irradiation was started and ceased, respectively.

The number of ADC counts in all four channels decreased very slightly during the first three days of irradiation. Then, after the chip had received a total dose of about 9 krad, radiation effects were observed.

In each of the pedestal channels (0 & 2), the number of ADC counts increased suddenly by about 10%, and then decreased steadily for the next four days. Then, after Chip D had received a total dose of about 17 krad, the number of ADC counts in each pedestal channel decreased very rapidly until both channels were reading zero. Irradiation was ceased shortly thereafter.

In each of the voltage channels (1 & 3), the number of ADC counts dropped suddenly by about 9%, and then increased fairly rapidly, leveling off at approximately

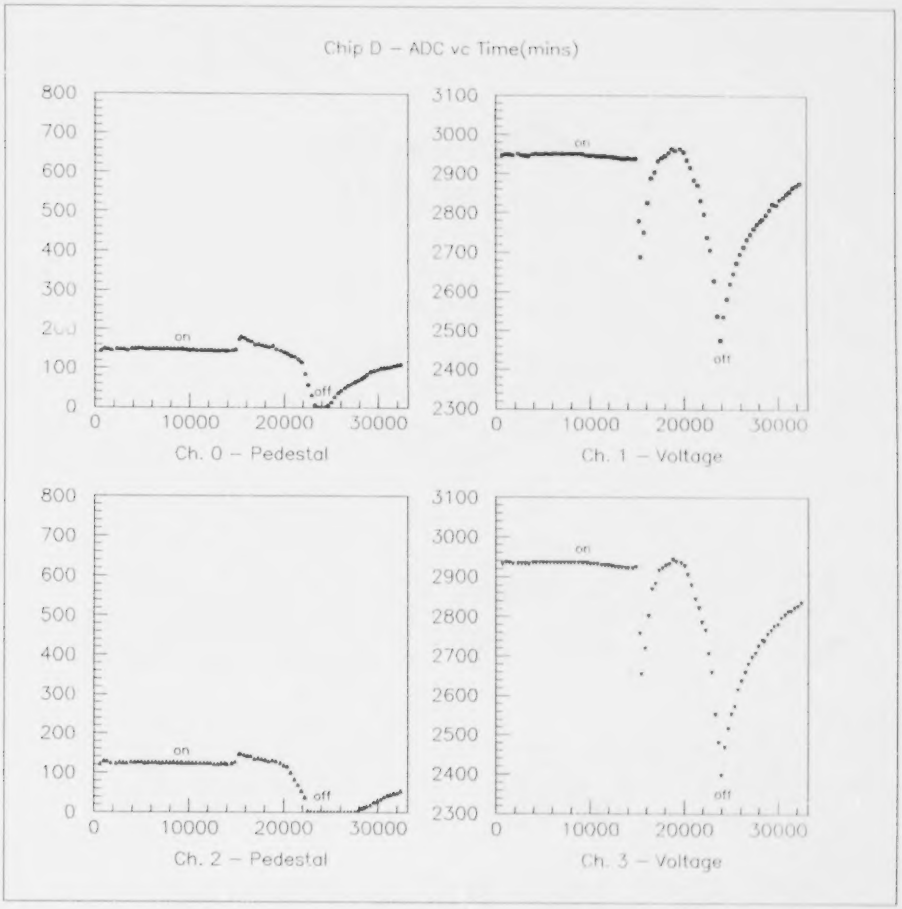

Figure 8.11: Mean number of ADC counts versus time (minutes) for Chip D.

the original value. Then, after Chip D had received a total dose of 15 krad, the number of ADC counts in each of the voltage channels decreased rapidly until irradiation was ceased.

After irradiation, Channel 0 soon recovered and the number of ADC counts increased steadily. The number of ADC counts in Channel 2 remained at zero for about 3 days, and then it too increased steadily. In voltage channels 1 and 3, the number of ADC counts immediately stopped decreasing and rapidly increased when irradiation was ceased.

Table 8.13 shows the number of ADC counts in each channel before irradiation, after three days of irradiation, after seven days of irradiation, and at the end of the run, for Chip D.

Channel	*Before Irradiation*	*After 3 Days of Radiation*	*After 7 Days of Radiation*	*At End of Run*
Ch. 0 - Pedestal	149.1	143.8	136.7	109.2
Ch. 1 - Voltage	2949.4	2938.2	2934.5	2875.8
Ch. 2 - Pedestal	125.6	121.4	115.2	53.7
Ch. 3 - Voltage	2935.1	2921.6	2905.3	2836.0

Table 8.13: Number of ADC counts for all four channels at various points in the run, for Chip D.

Table 8.14 shows the minimum and maximum number of ADC counts achieved during the entire run for all four channels.

A plot of the noise versus time (minutes) for the entire run with Chip D is

shown in Figure 8.12 for all four channels. Each point represents the rms noise of a 500,000 event file recorded at the corresponding time.

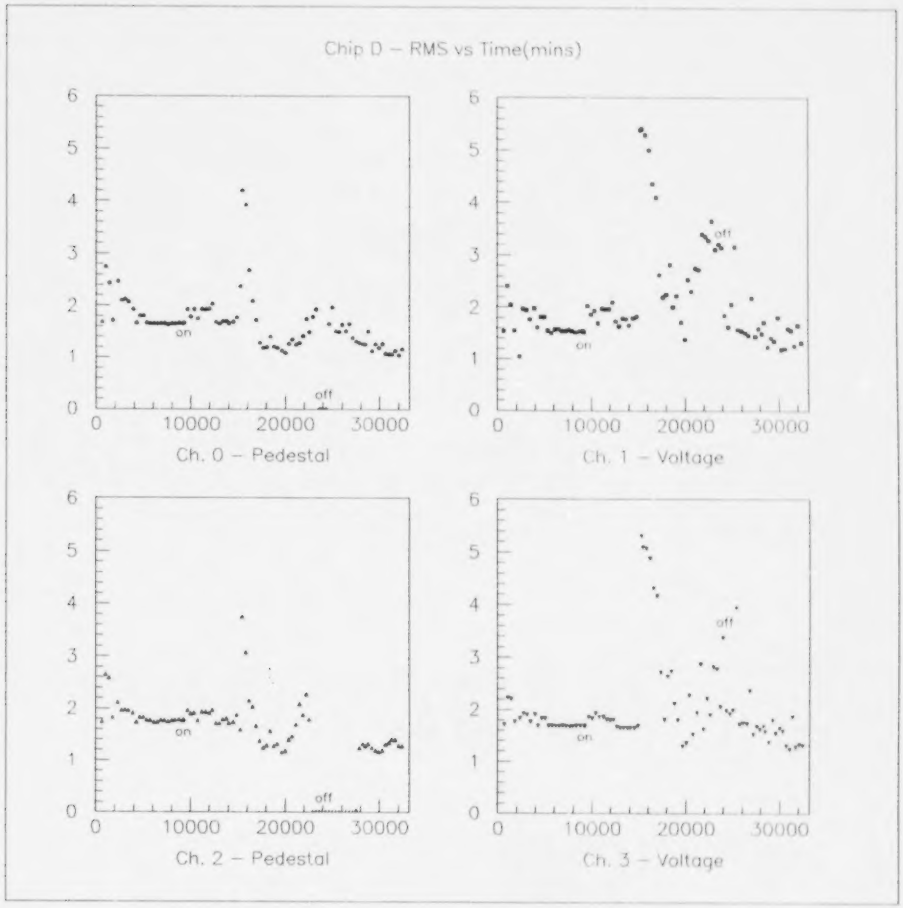

Figure 8.12: RMS noise (ADC counts) versus time (minutes) for Chip D.

The rms noise in all four channels was fairly steady prior to irradiation, at about 1.6 to 1.8 ADC counts. When irradiation is commenced, the rms noise increased by 0.2 ADC counts in all four channels. After 1.5 days of irradiation, the rms noise in each channel returned close to its original value. After three days of irradiation,

the rms noise in each channel suddenly increased to around 4 or 5 ADC counts, but then steadily decreased to values as low as 1.2 ADC counts.

In each of the pedestal channels (0 & 2), the rms noise remained near 1.2 ADC counts for more than one day, and then increased until irradiation was ceased. When the pedestal channels recovered, the rms noise in Channel 0 was initially 1.6 ADC counts, and decreased steadily to 1.2 ADC counts, while in Channel 2, the rms noise remained around 1.3 ADC counts

In each of the voltage channels (1 & 3), the rms noise did not remain at 1.2 ADC counts and increased until irradiation was ceased. Ending irradiation caused the rms noise in the pedestal channels to drop to about 1.8 ADC counts, and they decreased slightly until the end of the run.

Table 8.15 shows the rms noise in ADC counts in each channel before irradiation, after 3 days of irradiation, after 7 days of irradiation, and at the end of the run, for Chip D.

Table 8.16 shows the minimum and maximum rms noise achieved during the entire run for all four channels.

Throughout the entire run with Chip D, the air temperature within the lead shielding was 23 or 24 degrees Celsius.

8.2.6 Individual Cells

The mean ADC values represent not only an average over the events, but also an average over the 256 cells (capacitors) in each channel. Therefore, it is important to know if the radiation affected some cells more than others.

Channel	*Minimum*	*Maximum*
Ch. 0 - Pedestal	0.0	180.3
Ch. 1 - Voltage	2475.8	2963.2
Ch. 2 - Pedestal	0.0	147.3
Ch. 3 - Voltage	2398.4	2943.6

Table 8.14: Minimum and maximum number of ADC counts achieved during the entire run, for Chip D.

Channel	*Before Irradiation*	*After 3 Days of Radiation*	*After 7 Days of Radiation*	*At End of Run*
Ch. 0 - Pedestal	1.66	1.66	1.09	1.16
Ch. 1 - Voltage	1.54	1.65	1.38	1.32
Ch. 2 - Pedestal	1.76	1.71	1.17	1.27
Ch. 3 - Voltage	1.68	1.64	1.36	1.31

Table 8.15: RMS noise in ADC counts for all four channels at various points in the run, for Chip D.

In order to study this for Chip A, the mean ADC values of each of the 256 cells for files 07252111, 07270114 and 07300251 were used. The difference in mean ADC value for each cell between files 07252111 and 07270114 was calculated. A plot of difference in mean ADC value versus cell number for all four channels is shown in Figure 8.13. Then, the difference in mean ADC value for each cell between files 07270114 and 07300251 was calculated, and a plot showing this was produced (Figure 8.14).

During the period between files 07252111 and 07270114, ADC values were dropping rapidly in the voltage channels, and this was presumed to be a result of the irradiation. Similarly, during the period between files 07270114 and 07300251, ADC values were increasing rapidly in the voltage channels. It is clear from Figures 8.13 and 8.14 that the values for some groups of cells changed more than others during these periods. However, most cells changed by approximately the same amount.

8.2.7 Radiation Damage Mechanism

There are two ways in which radiation may damage electronics, and in particular the switched capacitor array chip. One possibility is that a particle hits across a gate, and damages (*eg.* shorts out) the cell. However, in the tests described in this section, no cells were observed to fail, or to become significantly noisier than others. A more plausible way in which radiation damage occurs is through charge deposition. Tests that were performed on irradiated SCA chips indicate that the radiation effects that were observed are due to charge deposition in the area of the op amp (operational amplifier).

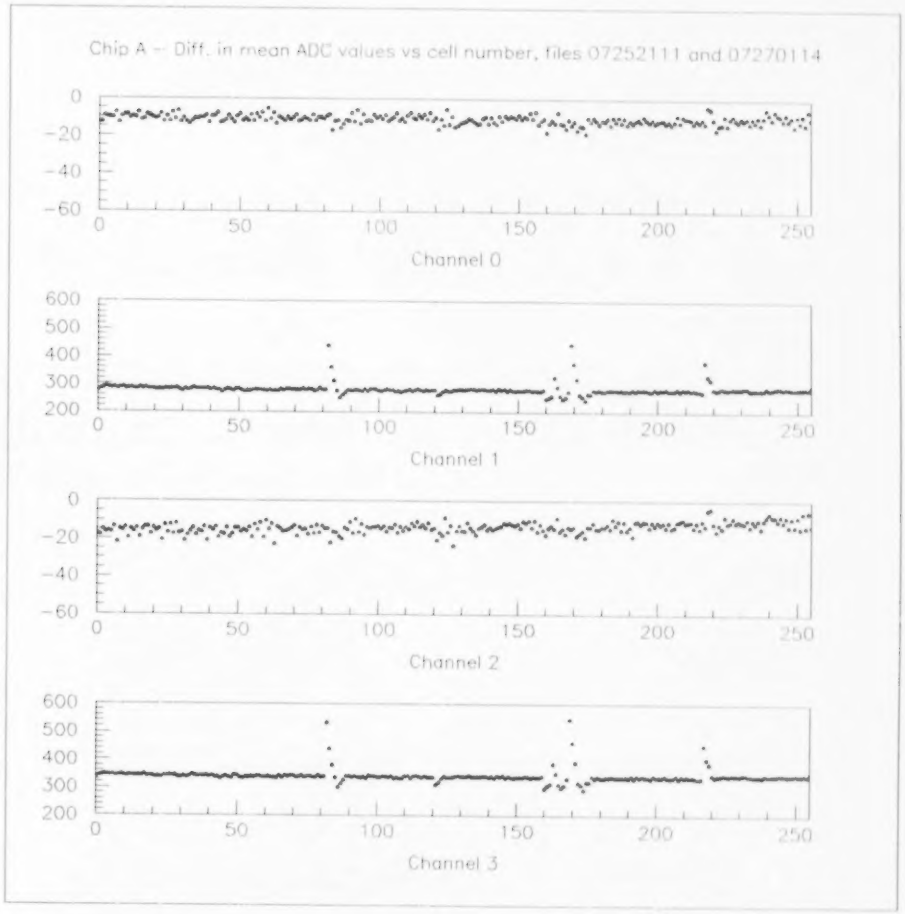

Figure 8.13: Difference in mean ADC values versus cell number between files 07252111 and 07270114 for all four channels.

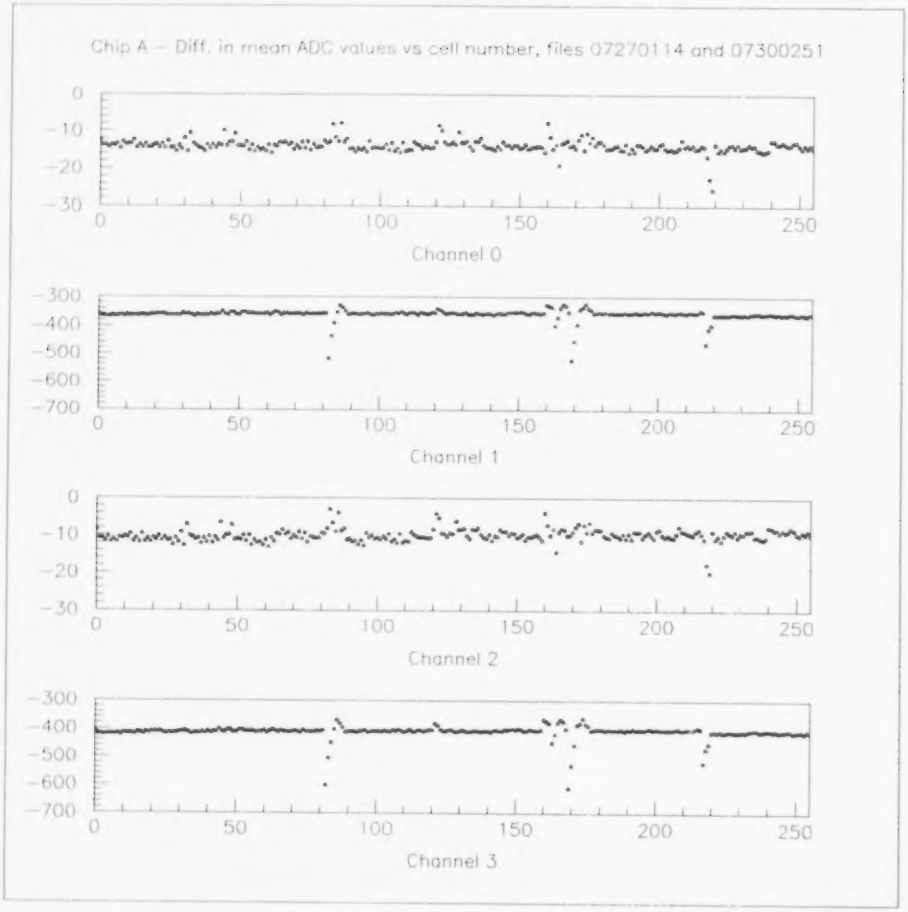

Figure 8.14: Difference in mean ADC values versus cell number between files 07270114 and 07300251 for all four channels.

8.2.8 Conclusions

Chip A performed well until it had received a total dose of 15 krad. At this point, the chip behaved erratically. Ceasing irradiation did not return the number of ADC counts in the four channels to their original values.

Chip B performed well until it had received a total dose of 15 krad. It also demonstrated erratic behavior at this point. After receiving a total dose of 29 krad, the number of ADC counts in all four channels of Chip B plummeted. Ending irradiation resulted in three of the four channels recovering somewhat.

So, it is concluded that the two chips failed at about the same total absorbed dose of radiation. Recall that Chips A and B were both placed the same distance (109 cm) from the source.

Chip C, however, was placed 57 cm from the source. Chip C performed well until it had received a total dose of 9 krad. After receiving a total dose of about 21 krad, the pedestal channels were dead, and the voltage channels were dropping rapidly. After irradiation was ended, three of the four channels recovered, although they did not return to their original values.

Finally, Chip D was placed 73 cm from the source. Chip D performed well until it had received a total dose of 9 krad. After receiving a total dose of about 17 krad, the pedestal channels were dead, and the voltage channels were dropping rapidly. After irradiation was ended, all four channels recovered well.

Table 8.17 summarizes the results of the exposure of SCA chips to gamma radiation.

In the ATLAS detector, the front-end electronics will be placed in the gaps between the barrel hadronic calorimeter and the extended barrel hadronic calorimeters.

Channel	*Minimum*	*Maximum*
Ch. 0 - Pedestal	1.05	5.40
Ch. 1 - Voltage	1.24	5.46
Ch. 2 - Pedestal	1.15	5.30
Ch. 3 - Voltage	1.24	5.19

Table 8.16: Minimum and maximum rms noise achieved during the entire run, for Chip D.

Chip	*Distance From Source*	*Dose Rate*	*Total Dose When Chip Shows Effects Due to Irradiation*
A	109 cm	81 rad/hour	15.3 krad
B	109 cm	81 rad/hour	14.7 krad
C	57 cm	113 rad/hour	8.6 krad
D	73 cm	86 rad/hour	8.7 krad

Table 8.17: Results of the photon irradiation of SCA chips.

Also, some front-end electronics will be located on the outer sides of the extended barrel hadronic calorimeters. Figure 8.15 shows the yearly integrated dose (Gy/yr) in the inner detector and the calorimeters. The expected maximum dose rates in these areas are 2.5 krad/year and about 0.1 krad/year, respectively. Thus, one would conclude that the SCA chips are not radiation hard enough to withstand 10 years of LHC operation, if the chips are located in the gaps between the barrel hadronic calorimeter and the extended barrel hadronic calorimeter.

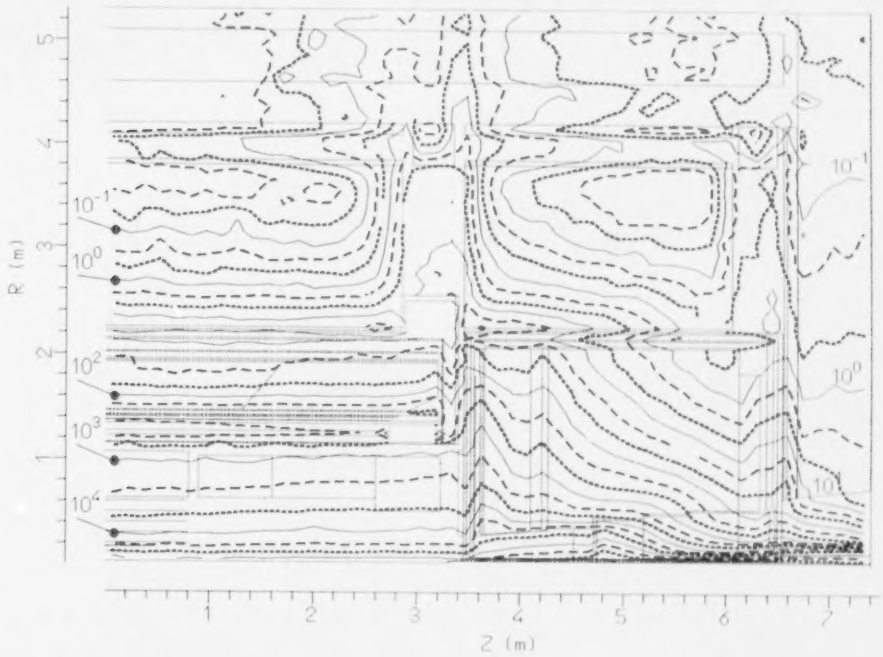

Figure 8.15: Yearly integrated dose (Gy/yr) in the inner detector and the calorimeters (taken from the ATLAS Technical Proposal, 1994).

Chips A and B showed effects after receiving 15 krad. Using this figure, SCA chips would survive 6 years of LHC operation at the location of higher dose rate. However, using the figures for Chips C and D (9 krad in both cases), SCA chips

would survive for less than 4 years. Chips A and B were located farther away from the source than Chips C and D in this test. It is possible that there is some recovery over time that allowed Chips A and B to endure a larger total dose without showing effects, due to a smaller dose rate.

A plot of dose rate versus elapsed time before effects are observed is shown in Figure 8.16. This plot does not follow a straight line, which is the reason for the suspicion that some recovery occurs as the SCA chips are irradiated. The expected dose rate at the LHC is much lower than the dose rate in this experiment, so it is conceivable that any recovery would allow the SCA chips to operate for longer than the above times.

The cause of the observed radiation effects is thought to be charge deposition in the area of the op amp.

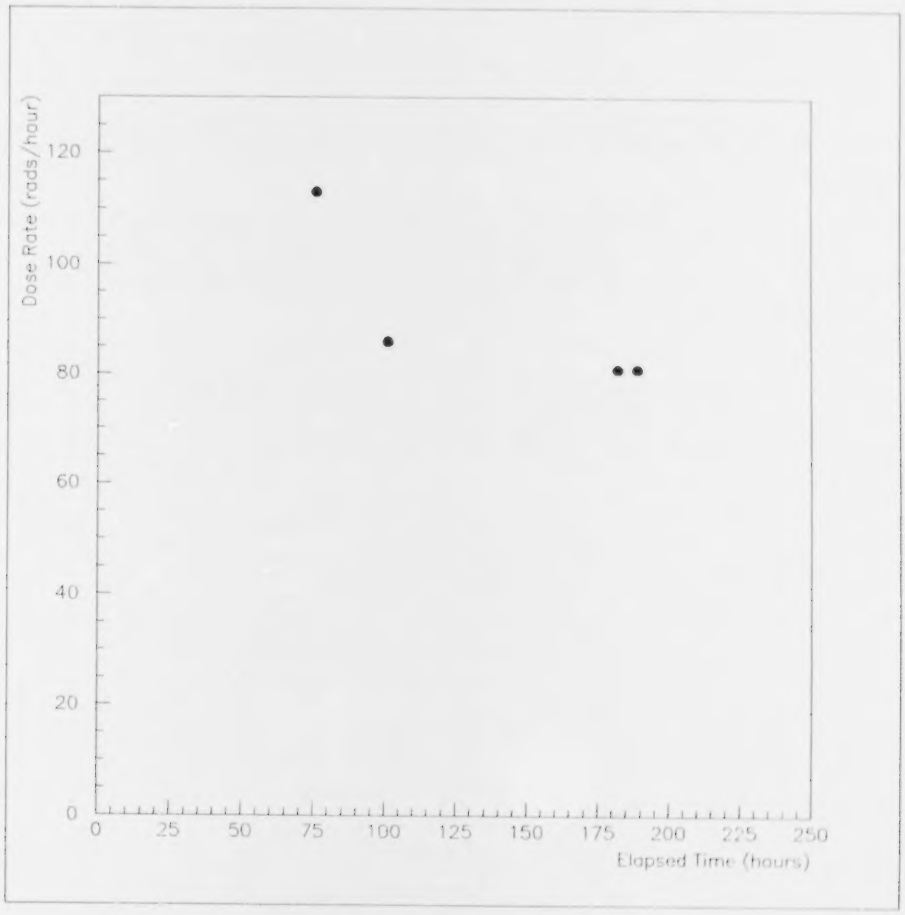

Figure 8.16: Dose rate (rad/hour) versus elapsed time (hours) to point where effects are observed, for gamma irradiation of SCA chips.

CHAPTER 9

Summary

The ATLAS detector will be used to explore the new energy regime that will become accessible with the operation of the LHC. Many physics issues may be studied by this general-purpose detector.

Due to the high rate of LHC proton-proton collisions, it is necessary to pipeline the signals from the calorimeter. An analog pipeline readout system for ATLAS calorimetry has been designed. Results indicate that this system, based on switched capacitor array (SCA) chips, will meet the ATLAS fast-electronics requirements. The readout system will accept input signals at a rate of 40 MHz, and will have a greater than 15-bit dynamic range. Several tests have been performed to determine the noise, radiation sensitivity and general viability of the SCA chips, and the results have been presented.

The noise of the SCA chip dictates the precision with which measurements can be made, and so is of great interest. It has been determined that the noise of the SCA chip is between 1.0 and 1.4 ADC counts over a full range of 4096 ADC counts. This is a fairly good result, and continued modifications to the SCA design will decrease the noise.

The performance of SCA chips when exposed to proton, electron and gamma radiation has been documented. The results of exposure to gamma radiation indicate that the current version of the SCA is not radiation hard enough to withstand ten

years of data-taking at the high luminosity of the LHC, unless considerable recovery were to occur.

Overall, the results are promising. With continued SCA chip improvements and general system modifications, an analog pipeline readout system which will meet the ATLAS requirements can be assembled.

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Appendix A

Estimating Coherent Noise Using Alternate Sums

Let the measurement of the value j (where j represents a certain channel), for event k be given by x_{jk}. Let $0 < j < M$ and $0 < k < N$. Then we can define:

$$x_{jk} \equiv \mu_j + a_k + b_{jk},$$

where

$$\mu_j \equiv \frac{1}{N}\sum_k x_{jk},$$

a_k is the coherent noise for event k which is the same over all channels, and b_{jk} is the random incoherent noise for event k and measurement value j.

By the above definitions,

$$\sum_k a_k = \sum_k b_{jk} = \sum_k a_k b_{jk} = \sum_{k,i\neq j} b_{jk} b_{ik} = 0.$$

Consider the pedestal subtracted sum of values over the channels:

$$S_k^+ = \sum_j (x_{jk} - \mu_j) = \sum_j (a_k + b_{jk}) = M a_k + \sum_j b_{jk}.$$

Consider the pedestal subtracted alternate sum of values over the channels:

$$S_k^- = \sum_j (-1)^j (x_{jk} - \mu_j) = \sum_j (-1)^j (a_k + b_{jk}) = \sum_j (-1)^j b_{jk}.$$

Now estimate the errors σ_+ and σ_- on the sum S_k^+ and alternate sum S_k^- using

$$\sigma_+^2 = \frac{1}{N-1}\sum_k (S_k^+)^2,$$

$$\sigma_-^2 = \frac{1}{N-1}\sum_k (S_k^-)^2.$$

Then, consider the difference

$$\begin{aligned}
\sigma_+^2 - \sigma_-^2 &= \frac{1}{N-1}\left[\sum_k (Ma_k + \sum_j b_{jk})^2 - \sum_k (\sum_j (-1)^j b_{jk})^2\right] \\
&= \frac{1}{N-1}\left[\sum_k (M^2 a_k^2 + 2Ma_k \sum_j b_{jk} + (\sum_j b_{jk})^2)\right. \\
&\quad \left. - \sum_k (\sum_j (-1)^j b_{jk})^2\right] \\
&= \frac{1}{N-1}\left[M^2 \sum_k a_k^2 + 2M \sum_j (\sum_k a_k b_{jk})\right. \\
&\quad \left. + \sum_k ((\sum_j b_{jk})^2 - (\sum_j (-1)^j b_{jk})^2)\right].
\end{aligned}$$

Now $\sum_k a_k b_{jk} = 0$, so

$$\begin{aligned}
\sigma_+^2 - \sigma_-^2 &= \frac{1}{N-1}\left[NM^2 < a^2 > + \sum_k (\sum_j b_{jk}^2 + 2\sum_{i \neq j} b_{jk} b_{ik}\right. \\
&\quad \left. - \sum_j b_{jk}^2 - 2\sum_{i \neq j} (-1)^i b_{jk} b_{ik})\right],
\end{aligned}$$

where $< a^2 > \equiv \frac{1}{N}\sum_k a_k^2$, the mean value of a_k.

Since $\sum_j b_{jk}^2 = 0$, one obtains

$$\sigma_+^2 - \sigma_-^2 = \frac{1}{N-1}\left[NM^2 < a^2 > + 4\sum_k \sum_{i \neq j, i \text{ odd}} b_{jk} b_{ik}\right].$$

Finally, $\sum_{k,i\neq j} b_{jk}b_{ik} = 0$, so

$$\sigma_+^2 - \sigma_-^2 = \frac{N}{N-1} M^2 < a^2 > .$$

Now, using $< a^2 > \equiv \sigma_{coh}^2$, one obtains

$$\sigma_+^2 - \sigma_-^2 = \frac{N}{N-1} M^2 \sigma_{coh}^2.$$

Thus,

$$\sigma_{coh} = \sqrt{\frac{N-1}{N}} \frac{\sqrt{\sigma_+^2 - \sigma_-^2}}{M}$$

$$\sigma_{coh} \approx \frac{\sqrt{\sigma_+^2 - \sigma_-^2}}{M}.$$

This is the equation which is used to estimate the coherent noise across channels of a data sample.